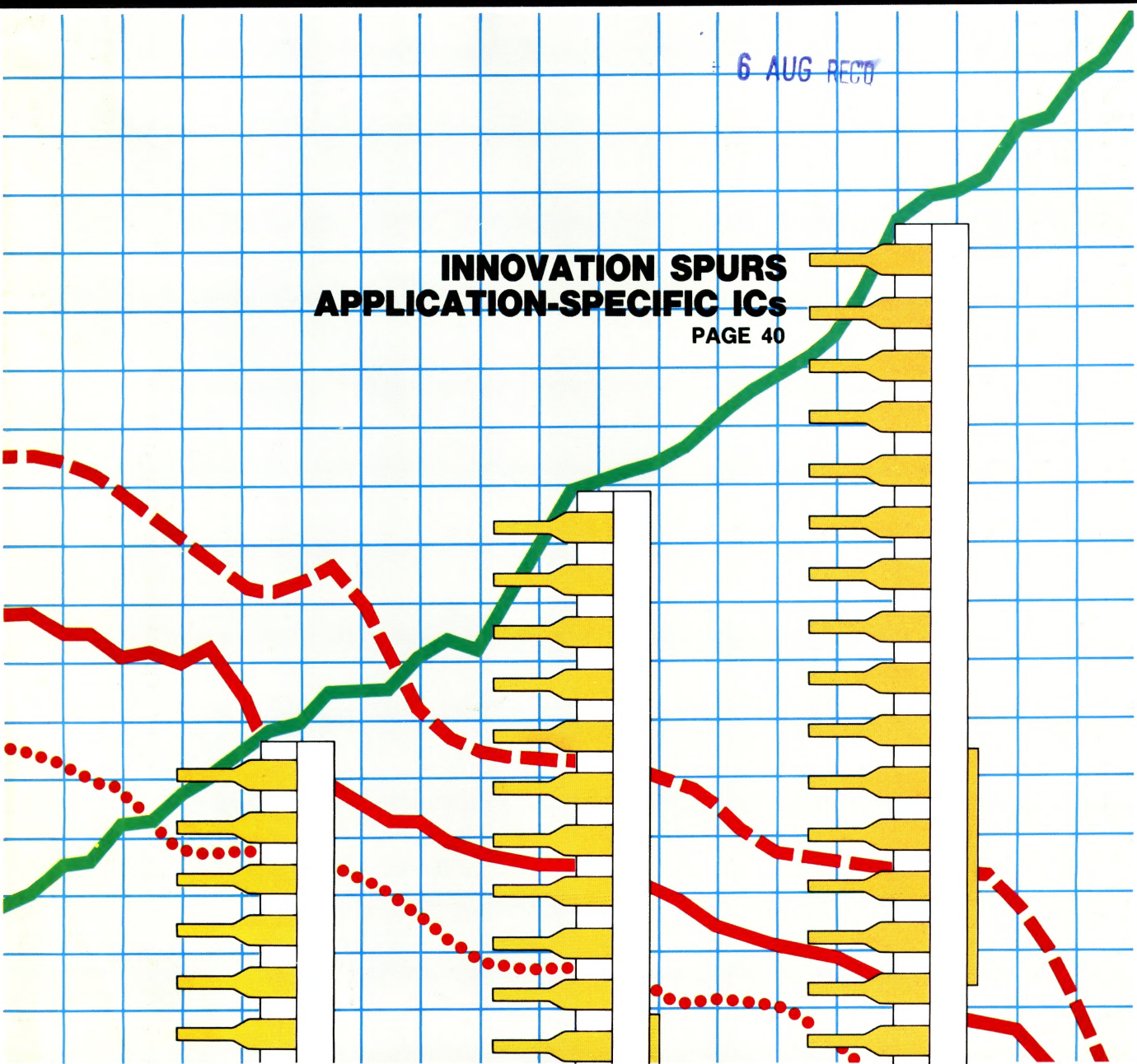


Electronics

THE WORLDWIDE TECHNOLOGY WEEKLY

JULY 22, 1985

A CHIP BUSINESS THAT'S STILL GROWING



IN HARD TIMES, A NEW ROLE FOR VENTURE CAPITAL/28
WILL A FRENCH 'STAR WARS' BEEF UP EUROPEAN R&D? 30



UNIX IS A TRADEMARK OF AT&T BELL LABORATORIES. SERIES 32000 IS A TRADEMARK
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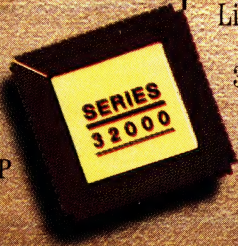
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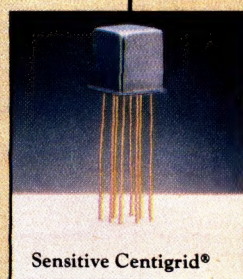
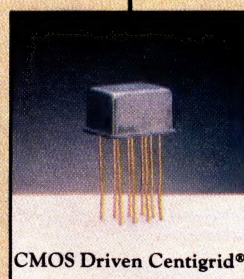
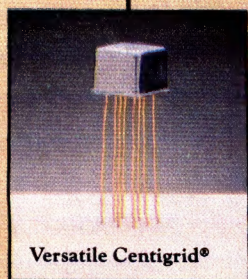


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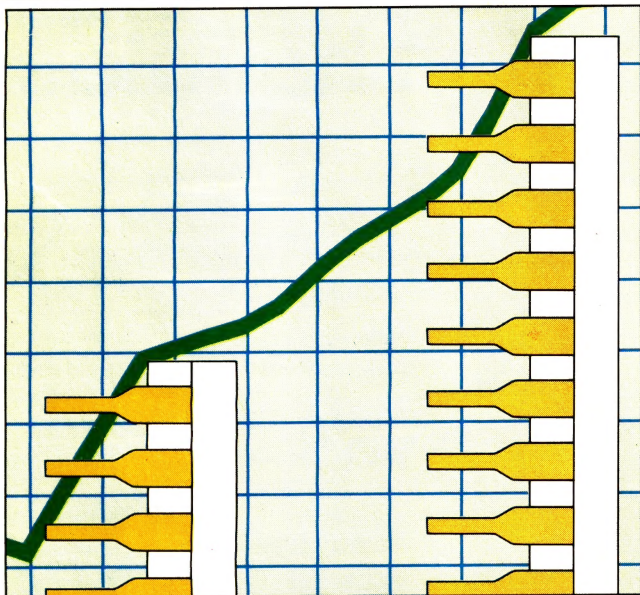
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Electronics

SPECIAL REPORT



COVER: A chip business that's still growing, 40

While the rest of the semiconductor industry struggles in one of the worst slowdowns in memory, makers of application-specific integrated circuits are enjoying healthy growth. As a result, innovations are cutting turnaround time and stretching chip design to unprecedented levels of complexity

Cover illustration by Gabor Kiss

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SIEMENS

PEB 2040 – a new dimension in switching networks

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Siemens has a new switching network device with unequalled capability, capacity and economy:

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The key to digital communication systems



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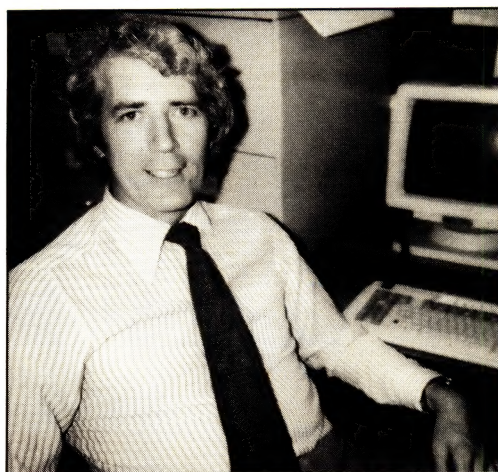
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There is always a problem when covering a conference: to try to tell all and say nothing or to pick one representative paper and report it well," says Kevin Smith, our senior editor in London. "The latter alternative often works better, because the other stories generally turn up again anyway."

But when Smith spotted a paper from Brunel University at the wafer-scale-integration workshop in Southampton earlier this month, he thought he had managed to capture the best of both alternatives, "because the paper's approach is sufficiently general purpose to tackle a wide class of tasks." Also, in Kevin's view, the technique described by the Brunel researchers (see p. 20) was one answer to the challenge of finding a wafer-scale application that would provide a commercial entry point.

It is especially appropriate for Charlie Cohen to write about Japanese consumer electronics technology, as he does in this issue on p. 21. Charlie, who has been reporting from Tokyo for *Electronics* for more than two decades, has chronicled the fortunes of the Japanese electronics industry since the heady days of the transistor radio.

His latest story, on enhanced-definition TV, takes him full circle. Charlie vividly recalls his early days in Tokyo, when NTSC color broadcasting had already started in the U.S. but monochrome TV broadcasting was still in its infancy in Japan.



Choices. Smith, in London, picks the right paper.

"The event that really put sales of the then-standard 14-in. black and white sets in high gear was the marriage of the crown prince in 1959. I watched that on my landlord's set."

Cohen at the time was studying for his MSEE at the University of Tokyo. Since going to work for *Electronics*, he has reported on many of the significant advances in the consumer, semiconductor, and computer industries. All these areas, he believes, will come together in the upcoming generation of enhanced and high-definition TV.

"It is ironic that the many U.S. engineers who deserted the consumer electronics field for the more glamorous computers created the market that pulled down the price of the memory chips that are needed to improve TV quality," says Charlie.

Laurence Altman

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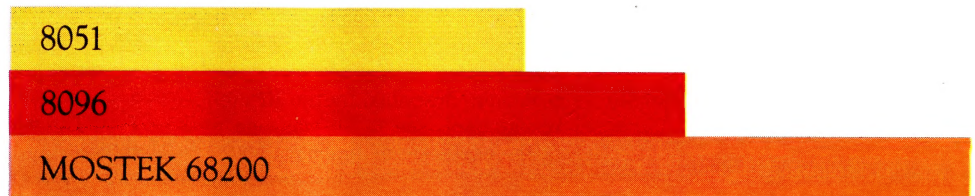
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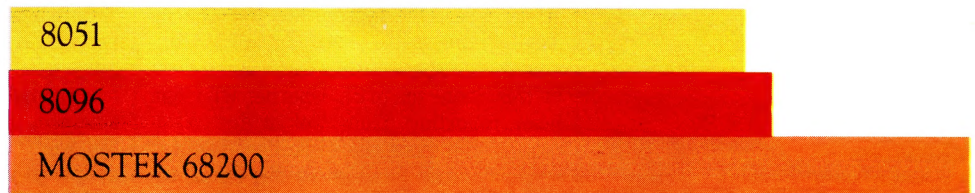
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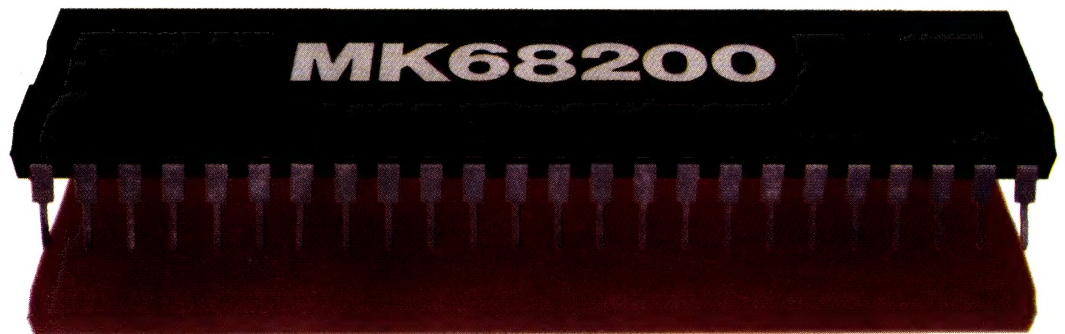
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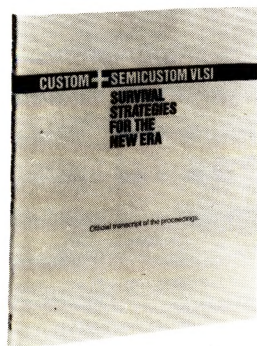
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MEETINGS

Federal Computer Conference, National Council for Education on Information Strategies (Michael Sullivan-Trainor, P.O. Box N, Wayland, Mass. 01778), Convention Center, Washington, Sept. 9-11.

Compint '85—Computer Aided Technologies Conference, IEEE (Stephen G. Leahey, P.O. Box 577, Desjardins Postal Station, Montreal, Quebec H5B 1B7, Canada) Palais des Congres, Montreal, Sept. 9-12.

Seventh Electrical Overstress/Electrostatic Discharge Symposium, Illinois Institute of Technology Research Institute and the EOS/ESD Association (Michael E. Martin, Publicity Chairman, 3M/Static Control Systems Division, 2111 W. Braker La., Building 501, Austin, Texas 78769-2963), Radisson South Hotel, Minneapolis, Sept. 10-12.

Midcon/85, IEEE *et al.* (Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, Calif. 90045), O'Hare Exposition Center, Chicago, Sept. 10-12.

Ineltec '85—International Exhibition of Electronics and Electrical Engineering, Swiss Industries Fair (CH-4021, Basel, Switzerland), Swiss Industries Fair, Basel, Sept. 10-14.

Swissdata '85—the Exhibition for Data Processing in Industry, Technical Application and Research, Swiss Industries Fair (CH-4021, Basel, Switzerland), Swiss Industries Fair, Basel, Sept. 10-14.

Mid-Atlantic Electronics Design and Production Expo, International Marketing Services Ltd. (1719 S. Clinton St., Chicago, Ill. 60616), Valley Forge Convention Center, King of Prussia, Pa., Sept. 11-12.

Third Computer Vertical Markets Conference, Frost & Sullivan Inc. (106 Fulton St., New York, N.Y. 10038), Stouffer's Inn, White Plains, N.Y., Sept. 12-13.

Canadian Independent Telephone Association Conference, Canadian Independent Telephone Association (Edmonton Telephones, P.O. Box 20500, Edmonton, Alberta T5J 2R4, Canada), Convention Centre, Edmonton, Sept. 16-18.

Data Storage '85, Disk/Trend Inc. and Freeman Associates Inc. (Cartlidge & Associates Inc., 1101 S. Winchester Blvd., San Jose, Calif. 95128), Red Lion Inn, San Jose, Sept. 16-18.

ICC '85 West—International Industrial Controls Conference and Exhibition, Tower Conference Management Co. (331 W. Wesley St., Wheaton, Ill. 60187), Long Beach Convention Center, Long Beach, Calif., Sept. 16-18.

Finishing '85 Conference and Exposition, Association for Finishing Processes of the Society of Manufacturing Engineers (1 SME Dr., Dearborn, Mich. 48121), Cobo Hall, Detroit, Sept. 16-19.

Fabtech International—Conference and Exposition for Metal Forming & Fabricating Technology, American Fabricating Institute of Technology and the Society of Manufacturing Engineers (SME, 1 SME Dr., Dearborn, Mich. 48121), McCormick Place West, Chicago, Sept. 16-19.

FOC/LAN '85, International Fiber Optic Communications & Local Area Networks Exposition, Information Gatekeepers Inc. (Joan Barry, Information Gatekeepers, 214 Harvard Ave., Boston, Mass. 02134), Brooks Hall/Civic Auditorium, San Francisco, Sept. 16-20.

Technology of Computer-Integrated Manufacturing, Computer-Integrated Manufacturing Systems (4 Main St., Los Altos, Calif. 94022), Sunnyvale Hilton, Sunnyvale, Calif., Sept. 17.

SEMINARS

Teleconferencing: New Developments for the Decade Ahead, Institute for Graphic Communication (IGC, 375 Commonwealth Ave., Boston, Mass. 02115), Andover Inn, Andover, Mass., Aug. 11-13.

Personal Microcomputer Interfacing and Scientific Instrument Automation, Virginia Polytechnic Institute and State University (Donaldson Brown Center for Continuing Education, Virginia Tech, Blacksburg, Va. 24061-0102), Virginia Tech Graduate Center, Falls Church, Va., Aug. 22-24; Airport Hilton Inn, Greensboro, N.C., Sept. 19-21.

Advanced Concepts of Color and Color Measurement, Rochester Institute of Technology (Technical and Education Center of the Graphic Arts, RIT, 1 Lomb Memorial Dr., Rochester, N.Y. 14623), Munsell Color Science Laboratory, RIT, Rochester, Aug. 26-28.

Laser Safety: Inspection & Control, Laser Institute of America (5151 Monroe St., Toledo, Ohio 43623), Terrace Hilton, Cincinnati, Sept. 16-20.

THIS **Electronics** WEEK**THURSDAY** July 11

The Semiconductor Industry Association said **a slight shipping increase, coupled with an order decrease in June, produced a book-to-bill ratio of 0.72 : 1 for chip makers** for the second straight month. U.S. market sales totaled \$725.6 million for June, up 1.5% from May, but orders slipped 4.1% from May and 57.4% from a year ago. . . . National Semiconductor Corp., one of the companies hit hardest by this year's chip-industry slump, said that Sandia National Laboratories, Albuquerque, N.M., will develop **a family of radiation-hardened microprocessors based on National's 32000 family of 32-bit products**. Sandia will design and manufacture five CMOS chips with technical assistance from National.

FRIDAY July 12

Second-quarter earnings reports began to come in, with some major industry players reporting huge, if not surprising, declines. **Earnings at Motorola Inc. dipped by more than 70%** as the Schaumburg, Ill., company reported earnings of just \$26 million, compared with \$98 million a year ago. . . . Motorola was not the only company showing poor results. **United Technologies Corp. reported a 68% decline for the second quarter**. UTC, Hartford, Conn., declared a net income of \$54.8 million, compared with 1984's \$168.9 million. It blamed the dive on Mostek Corp., its struggling semiconductor and systems unit in Carrollton, Texas, saying that without that division, earnings for the first two quarters of 1985 are ahead of 1984's figures.

MONDAY July 15

As the 13th National Computer Conference opened in Chicago to smaller crowds than in previous years, **IBM Corp. said earnings were off 12.9%, to \$1.4 billion**, in the second quarter. The computer giant blamed its poor performance on a combination of slowing mainframe sales in anticipation of the long-awaited Sierra, or 3090, mainframe computer, the strength of the dollar overseas, and the "soft U.S. economy." Delivery of the Sierra, on which rest the company's hopes for renewed vigor in the second half, will begin in the third quarter, three months ahead of schedule. . . . Not everyone is doing badly, however. **E-Systems Inc., Dallas, is having a record year in defense-electronics sales and a near-record year in backlogs**. E-Systems' revenues of \$238 million in the second quarter top its previous three-month sales record of \$220 million in this year's first quarter.

TUESDAY July 16

The Communications Workers of America said a study conducted by its locals in North Carolina indicates that **workers who regularly use video display terminals for their jobs may show a significantly higher incidence of angina**, or chest pains, than is found in the general population. The group said its locals studied 1,000 VDT users in the telecommunications industry and found that about 18% complained of angina, compared with a normal incidence of about 3%.

WEDNESDAY July 17

Bucking the industry trend, **Sperry Corp. reported that its fiscal first-quarter net earnings leaped 156% from a year ago**, giving it a profit of \$51.5 million. The New York company was able to eclipse last year's figure mostly because of a large 1984 first-quarter writedown. Excluding the writedown, Sperry's earnings still grew by 21.8%. □

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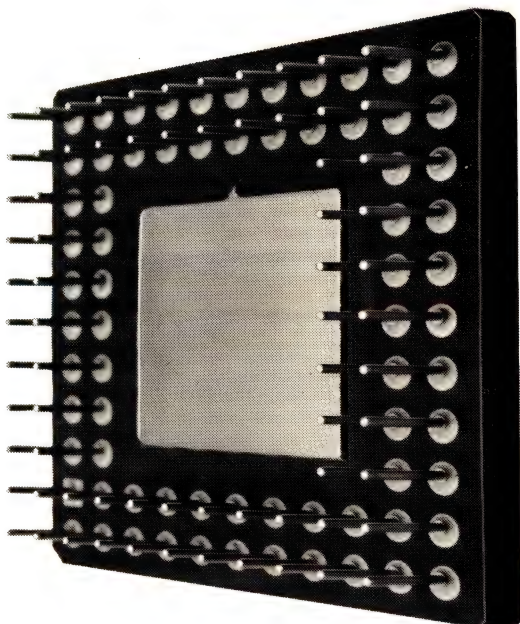


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ELECTRONICS NEWSLETTER

JAPAN IC EXPORTS TO U.S. DOWN 32% IN FIRST FIVE MONTHS OF 1985

Japanese exports of integrated circuits to the U.S. for the first five months of 1985 are down 31.8% from the same period last year, according to recent statistics from the Ministry of Finance. Total exports were \$379 million in the face of the slumping U.S. personal computer market. U.S. IC exports to Japan also decreased to \$218 million from January to May this year, a drop of 22.2%. For the whole year, the ministry expects Japanese IC exports to the U.S. to total about \$1.41 billion, 10% lower than in 1984. □

TEXAS INSTRUMENTS TO DEMONSTRATE COLOR-GRAPHICS CHIP AT SIGGRAPH

Demand for color-graphics chips remains one of the few bright hopes in an otherwise dismal integrated-circuit business. Therefore, industry observers are expecting that silicon makers will reverse a 1985 trend and make a stronger than usual trade-show appearance at this week's Siggraph '85 in San Francisco. Texas Instruments Inc. plans to provide an advance peek at what will eventually become a new video-palette product, the 22-pin TMS34070. The Dallas company is aiming its chip at personal computers and low-cost work stations. It integrates digital-to-analog converters, analog interfaces, and a color lookup table to provide a 4-bit color-palette code to display 16 out of 4,096 available colors at a time on each line. The 34070's lookup table can be changed line-by-line to enhance the images, and it will work at 36 MHz—or up to 800 by 600 pixels, noninterlaced—with 10-ns rise and fall times at the red-green-blue output. Without host-processor intervention, the palette will also load itself directly from memory. Inmos Corp., Colorado Springs, is expected to introduce a similar color lookup table, the 28-pin IMSG170. The Inmos device also integrates three on-chip DACs and a micro-processor bus interface. □

IEEE COMMITTEE DEFINES TWO PROTOCOLS FOR NETWORKING PROCEDURES

The local-area-network standards committee of the Institute of Electrical and Electronics Engineers is working out a compromise between those two traditionally antithetical packet-switching protocols—datagrams and virtual circuits—in setting up its internetworking procedures. The 802 committee will define both protocols, said chairman Maris Graube after this month's meeting in Vancouver, B.C. This will give users a choice according to their application needs. For applications that use the LAN as a multiplexer, such as connecting terminals and personal computers to wide-area networks, the X.25 virtual-circuit protocol may be preferable; datagrams could find favor in networks at a single site.

Having gained IEEE approval of its main-link and physical-layer protocols, the committee continued to nail down minor issues at Vancouver. It began coordination of network-management protocols for monitoring and adjusting performance conditions. One subcommittee voted not to accept the proposed 2-Mb broadband standard for collision sensing and multiple access with collision detection, which would have put Ethernet into broadband form.

As an indication of the growing importance of the Manufacturing Automation Protocol (MAP) factory-automation system initiated by General Motors Corp., subcommittee 802.4 formed no less than a dozen subgroups to investigate various aspects of the token-bus protocol, MAP's bottom two layers. Further emphasizing the importance of MAP to him, Graube said after the meeting that he plans to leave Tektronix Inc., where he has headed an internal standards group, to devote all his time to the multisupplier MAP system. He will form a MAP consulting firm—Shipstar Associates—with Robert Crowder, chairman of an American National Standards Institute committee on factory automation—and will continue to chair 802. □

ELECTRONICS NEWSLETTER

IBM VOICES SUPPORT FOR HIGHER LAYERS OF OSI MODEL

Anouncing its commitment to OSI, IBM Corp. last week said it plans to develop products compatible with the higher layers of the open-systems-interconnection reference model fostered by the International Organization for Standardization and the International Telephone and Telegraph Consultative Committee. IBM will also set up a European networking center in Heidelberg, West Germany, to work on OSI research.

This is the first time that IBM has stated publicly that it would support the upper layers of the OSI model. The company leaves itself a loophole, however, by adding that it would still evaluate layers six (presentation) and seven (application) as they become available. It plans to develop products compatible with the standards "based on business considerations." IBM has been under pressure from member countries of the European Communities to offer OSI-compatible products [*ElectronicsWeek*, Feb. 25, 1985, p. 35]. □

TOSHIBA LICENSES SIEMENS TO MAKE 1-Mb CMOS DRAM

Toshiba Corp., Kawasaki, Japan, has licensed the technology for its next-generation 1-Mb CMOS dynamic random-access-memory chip to Siemens AG. In return for a license fee and royalties, the Munich company will sell the Toshiba parts on the world market. Toshiba started shipping engineering samples in June and doesn't expect to reach a production volume of 100,000 units until the middle of next year. Siemens could then start shipping samples next year, rather than in 1987 as it originally planned. The two companies also concluded a cross-licensing agreement on other devices, including power MOS FETs and large-scale integrated circuits for communications. Japanese government approval is needed. □

HUGHES SIGNS CONTRACT IN JAPAN'S SATELLITE MARKET

Hughes Communications Inc., a part of Hughes Aircraft Co., has become the first U.S. company to sign a major contract in Japan's newly deregulated satellite market. The El Segundo, Calif., electronics conglomerate pegs the value of its agreement with its Japanese joint-venture affiliate, Japan Communications Satellite Co., at more than \$300 million. The deal covers the launching and ground-system operation of two satellites. Hughes will launch the first satellite, a 32-transponder Ku-band system, in December 1987 using either a U.S. Space Shuttle or European Ariane booster rocket. Hughes will launch the second satellite in spring 1988. Hughes has a 30% share in Japan Communications Satellite, with the remainder owned by trading firms C. Itoh & Co. (40%) and Mitsui & Co. (30%). □

SMART-CARD TELEPHONES HIT THE MARKET

While makers of smart cards (credit cards with a microprocessor and memory) eagerly await the results of customer trial runs throughout the U.S., a new company is selling a line of telephones it believes is the first to use the European-developed technology in a domestic mass-market application. Multimil Inc., Richardson, Texas, this month got the go-ahead from the Federal Communications Commission to market the phone sets, which can store up to 1,000 telephone numbers on a single, removable smart card, called Memocard. The card, which contains 2-K bytes of electrically erasable programmable read-only memory, can also store telephone credit-account numbers. It was developed by the company's majority stockholder, Multimil International SA, Geneva, Switzerland. The telephone products include a \$585 add-on smart-card adapter that plugs into standard telephone sets. A fully integrated smart-card phone has a suggested retail price of \$685. □

This image shows a custom PCB for a Commodore 64, featuring a 74180 logic chip. The board is populated with several integrated circuits (ICs) and other components. Key components include:

- 74180:** A 16-bit parallel adder/subtractor, located in the center of the board.
- 74150:** A 4-to-16 decoder, located in the top right corner.
- 74151:** A 5-to-32 decoder, located in the top left corner.
- 74152:** A 4-to-16 decoder, located in the bottom left corner.
- 74153:** A 4-to-16 decoder, located in the bottom right corner.
- 74154:** A 4-to-16 decoder, located in the middle right section.
- 74155:** A 4-to-16 decoder, located in the middle left section.
- 74156:** A 4-to-16 decoder, located in the middle right section.
- 74157:** A 4-to-16 decoder, located in the middle left section.
- 74158:** A 4-to-16 decoder, located in the middle right section.
- 74159:** A 4-to-16 decoder, located in the middle left section.
- 74160:** A 4-to-16 decoder, located in the middle right section.
- 74161:** A 4-to-16 decoder, located in the middle left section.
- 74162:** A 4-to-16 decoder, located in the middle right section.
- 74163:** A 4-to-16 decoder, located in the middle left section.
- 74164:** A 4-to-16 decoder, located in the middle right section.
- 74165:** A 4-to-16 decoder, located in the middle left section.
- 74166:** A 4-to-16 decoder, located in the middle right section.
- 74167:** A 4-to-16 decoder, located in the middle left section.
- 74168:** A 4-to-16 decoder, located in the middle right section.
- 74169:** A 4-to-16 decoder, located in the middle left section.
- 74170:** A 4-to-16 decoder, located in the middle right section.
- 74171:** A 4-to-16 decoder, located in the middle left section.
- 74172:** A 4-to-16 decoder, located in the middle right section.
- 74173:** A 4-to-16 decoder, located in the middle left section.
- 74174:** A 4-to-16 decoder, located in the middle right section.
- 74175:** A 4-to-16 decoder, located in the middle left section.
- 74176:** A 4-to-16 decoder, located in the middle right section.
- 74177:** A 4-to-16 decoder, located in the middle left section.
- 74178:** A 4-to-16 decoder, located in the middle right section.
- 74179:** A 4-to-16 decoder, located in the middle left section.
- 74180:** A 4-to-16 decoder, located in the middle right section.

The board is populated with various other components, including resistors, capacitors, and a 74180 logic chip. The board is labeled with "COMMODORE 64" and "74180" in the top left corner. The board is also labeled with "74180" in the bottom right corner. The board is populated with various other components, including resistors, capacitors, and a 74180 logic chip.

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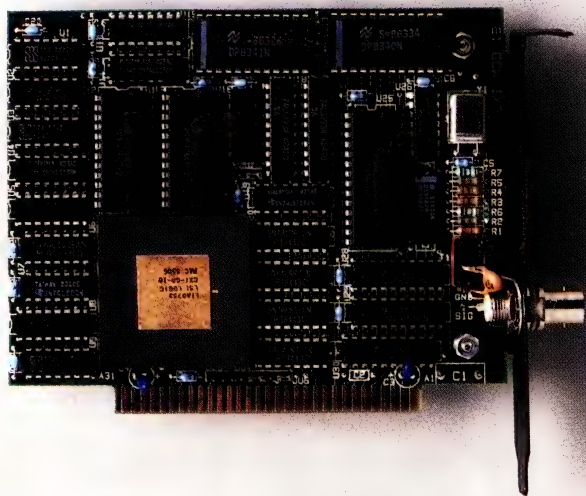
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Electronics

SUBTHRESHOLD FETS KEEP PACEMAKER BATTERIES ALIVE

Analog ICs operating below threshold voltage get by on ultralow currents

Freeport, Texas

Occasionally, design constraints work to a technology's advantage. A case in point is the extremely low currents required for analog circuits in programmable pacemakers. For operation at levels as low as 10 μm , engineers are devising CMOS chips that capitalize on the little-explored and rarely used weak-inversion region. The outcome is low-power chips that are easy to manufacture and have higher transistor gain, which can result in smaller dice.

In a MOS transistor, as the gate-to-source voltage rises from zero a depletion region begins to form on the channel's surface. This region grows thicker until the threshold voltage and a condition called effective or strong inversion is reached. Above this threshold voltage, relatively large currents will flow between source and drain and will have a square-law response to changes in gate voltage.

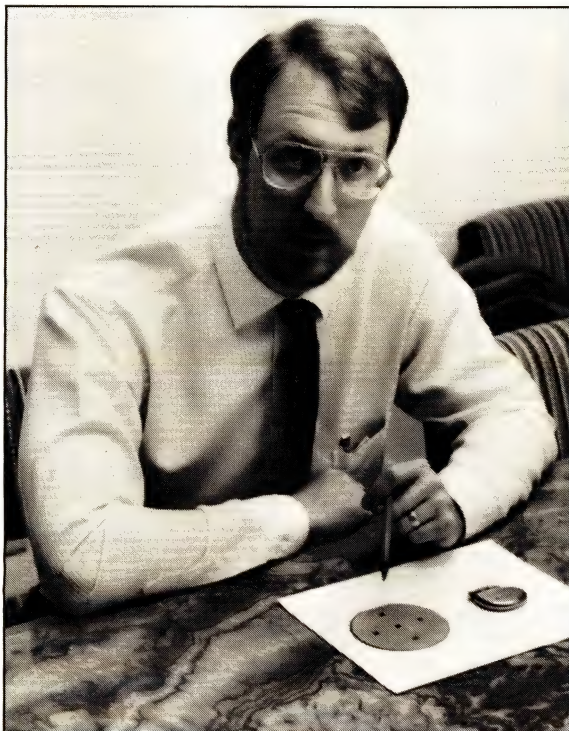
Engineers usually design transistors to operate in this strong-inversion area of their operating characteristics. But below the threshold voltage, in the weak-inversion region, tiny currents will flow, changing exponentially with gate voltage.

"The particular set of restrictions that we design integrated circuits to is also ideal for operating below the threshold turn-on voltage of MOS," explains Larry J. Stotts, IC-design group leader at Intermedics Inc. The pacemaker firm, like some of its leading U.S. competitors, develops many custom CMOS chips for implantable pacers and drug-delivery systems. Most of Intermedics' designs are fabricated by Zymos Corp., Santa Clara, Calif., which is 46% owned by the Freeport company.

Low currents—as little

as 10 μA for standby mode and about 40 μA during active pacing of the heart—are necessary to ensure longevity of the lithium-iodine batteries that power Intermedics' pacers, known as Cosmos [*Electronics*, March 10, 1983, p. 47]. They are based on 8-bit microprocessors. While developing large-scale analog chips for these ultralow currents, Intermedics engineers opted to keep CMOS transistors at a 5- μm size and work in the region below the threshold. Working above the threshold would require much smaller device structures and advanced semiconductor processing, which adds to costs.

Weak-inversion MOS transistors, operating with subthreshold voltages, demonstrated much higher gain than standard MOS designs, notes Stotts. The weak-inversion CMOS makes possible a voltage gain of 800 to 1,000 in a single-stage operational amplifier. The gain is roughly two orders of magnitude greater than that of standard single-stage CMOS op amps.



Limits. Operating transistors below their threshold voltages is ideal for pacemaker circuits, says Intermedics' Larry Stotts.

Stotts says the weak-inversion region's gain characteristics provide analog-IC designers greater flexibility. The result can be smaller dice—a critical requirement when attempting to embed more processing of sensor signals inside pacers to monitor the heart and body. Many of the custom chip designs are now doubling as intelligent controllers for implantable drug-delivery systems, which react to changes in the body and release medicine according to firmware-embedded instructions.

Though weak inversion is finding a home in the implantable medical electronics, subthreshold CMOS circuits are generally too slow for conventional equipment needs, says Michael J. Callahan, cofounder and executive vice president of engineering at Crystal Semiconductor Corp., Austin, Texas. Before starting Crystal, Callahan founded Texas Micro Engineering Co., which designed weak-inversion CMOS ICs for pacemaker firms.

Keep it cool. "You can do some pretty impressive things with weak inversion, but you cannot do it at high speeds or work in the high temperatures required outside the implantable medical systems industry," Callahan notes.

Intermedics uses weak-inversion structures in a low-voltage, low-current crystal oscillator recently integrated on a new 8-bit microcomputer, which operates at 100 kHz (a standby monitoring mode) to 2 MHz (the active heart-pacing mode) at 2.8 V. The company is using its chip, featured earlier this year at the International Solid-State Circuit Conference, inside a new line of Cosmos pacers.

The highly redundant Cosmos pacers generally contain a microprocessor, two large-scale ICs with both analog and digital circuits, and a custom static memory chip. The analog ICs monitor the heart and microprocessor, plus handle a radio-frequency link used by physicians to collect diagnostic data and to download new programs into memory. If the host 8-bit microprocessor produces errors, the analog circuits will override the system and take over heart-pacing duties.

—J. Robert Lineback

SLOW GaAs RAM COULD BE A WINNER

Limeil-Brévannes, France

A gallium arsenide memory chip developed at the Laboratoires d'Electronique et de Physique Appliquée (LEP) boasts neither the fastest access time nor the highest density yet reported for such chips. But because the chip should be easy to build, its developers think it may have the brightest future of any GaAs memory announced to date.

The circuit is a 1-K static random-access memory, the first such GaAs chip to be developed in Europe. Though two Japanese laboratories have produced 4- and 16-K

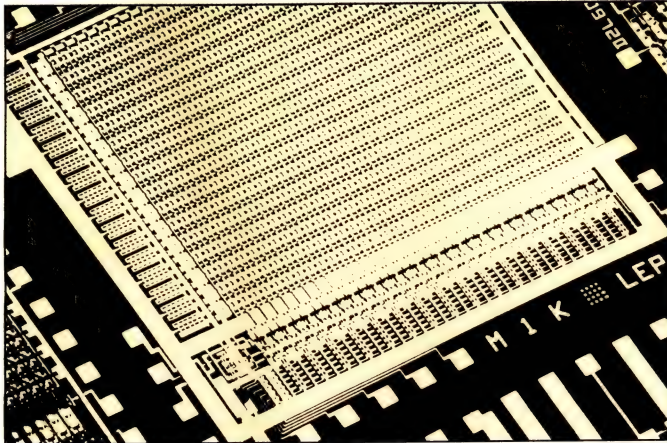
GaAs memories, researchers at LEP, the principal French research facility of Dutch multinational NV Philips, think their results at the more modest density could give them an edge in developing a high-volume product. Fifth-generation computers will create a demand for ultrafast caches—the small, fast storage buffers integrated in the central processing unit of some large computers.

At issue are two key criteria—power consumption and the ability to consistently reproduce a given chip. These figures often get less notice in evaluating laboratory results for GaAs chips than do flashier figures for propagation delay and, for memories, access time.

The LEP 1-K memory's access time is 3 ns with power consumption of 60 mW at room temperature. These are not record figures, but they compare favorably with the results announced for similar chips from the companies that LEP considers most advanced in GaAs memories—Nippon Telegraph & Telephone Public Corp. and Fujitsu Ltd.

Speed-power trade-off. NTT's chip can show an access time half that of the Philips lab's, but only at the cost of increasing the power consumption more than sixfold, to 370 mW. Fujitsu's 1-K memory is somewhat slower than the French chip, with a 3.4-ns access time for a significantly higher power consumption of 290 mW. Operated at liquid-nitrogen temperature, the Fujitsu circuit's access time drops to a blazing 0.9 ns, but at the cost of boosting its power consumption to the level of NTT's memory. NTT, Fujitsu, and LEP all fabricate their parts using 3- μ m design rules.

As for their chip's good reproducibility, the French researchers credit two factors. The first is that it uses a simple, five-step, normally-off metal-semi-



Fast European. A 1-K GaAs memory from the Laboratoires d'Electronique et de Physique Appliquée uses only 60 mW for an access time of 3 ns.

conductor FET process that requires about eight days to process a wafer. NTT uses a highly complex process based on direct-coupled FET logic that requires at least 40 days to complete a wafer.

One sign of the complexity of NTT's approach is that in its most successful 1-

K memory, just 98% of the memory cells operate as they should. LEP, however, is confident that it can reproduce its 100% operational chip with reasonable yields. Fujitsu uses a high-electron-mobility-transistor approach that is designed for optimal operation at 77 K. Since producing 1-K memories, both Japanese companies have developed 4-K circuits, and NTT has even announced a 16-K memory.

What LEP considers its other key advantage is the process it developed in-house for growing ingots of GaAs that are free of dislocations—imperfections in the semiconductor crystal that can degrade the performance of chips produced from it by creating high pinch-off voltages. LEP uses a liquid-encapsulation method with doping with elements from columns III and V of the periodic table, which yields 2-in. ingots that are free of dislocation.

—Robert T. Gallagher

BUSINESS ABROAD

VALUE-ADDED NETS LURE SWARM OF FIRMS IN JAPAN

Tokyo

Competition is getting fierce in the rush to exploit Japan's newest, but still undefined, market: value-added networks. Although the overall market for VAN services should grow eightfold, to more than \$800 million, over the next five years (see chart), nobody seems to have a handle on which services will be most lucrative. And the major players are vying for payoffs in both VAN equipment and services.

James Hubley, AT&T International's director of network services in Japan, says systems that link vendors with suppliers and buyers—providing tracking of purchase orders and invoices—is one big customer need. He lists such services as distribution-network control, credit-card authorization, and teleconferencing as other prime markets.

Nearly 150 companies have declared their intention to enter one form of VAN business or another. "That will be the big difference in this market," says John F. Barber, managing director of

General Electric Technical Services Co.'s Tokyo office. "In America, it's all big guys. But in Japan, the little VANs will play an important part in the market." The reason is that many Japanese companies will run their own in-house VANs because they feel more comfortable when they have total control of their information flow.

Liberalized by recently enacted telecommunications laws that ended the

common-carrier monopoly of Nippon Telegraph & Telephone Public Corp., Japan's VAN business splits into two broad types. According to new laws, Type 1 in-

cludes common carriers such as NTT and new groups like Daini-Denden Inc. [*ElectronicsWeek*, July 30, 1984, p. 43], which will compete with NTT along the busy Tokyo-Nagoya-Osaka-Kobe corridor using a microwave network. Type 2 groups, under new laws, must lease their lines from Type 1 companies.

The Ministry of Posts and Telecommunications (MPT) has approved five new Type 1 groups, including two satel-

*Computer firms
see nets yielding
a double payoff*

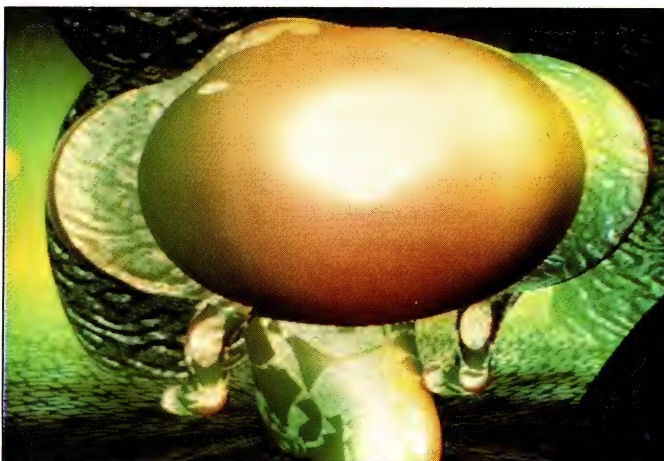
COMPUTERS IMITATE NATURE'S

If you can compute dirt, you're hot." That's how one exhibitor characterizes the state-of-the-art computer graphics—natural scenes including blurred motion and plant life—that will be in full flower this week at the Association for Computing Machinery's Siggraph '85 show in San Francisco. The exhibitor observes, "Shiny surfaces and ray tracings are out, particles and plants are in." The illustrations on these pages are from an art show that accompanies Siggraph, which includes a video animation from Lucasfilm Ltd., San Rafael, Calif.

Far right is "Knoll," by David Kamens of Boston University, a 20-by-20-in. print from an image he created on an IBM Corp. 3081-D and a Digital Equipment Corp. VAX with a Matrix Instruments Liacom display generator and BU Solids Modeling System software.

Growing grass. Near right top is "Quadric Clouds," a video image by Geoffrey Y. Gardner of the Grumman Research Center on a Data General Corp. Eclipse computer with a Genisco graphics controller. Next is "Growth III: Origin," by Yoichiro Kawaguchi of the art and sciences lab of Nippon Electronics College, Tokyo, done on the Links 1 multiprocessor at Osaka University using the Metaball algorithm. At the bottom is "Blowin' in the Wind: The Movie," by Bill Reeves of Lucasfilm, who used a VAX and his own rule-based Particle Systems algorithm. Reeves' grass was created by providing rules for grass growth, then letting the system draw it.

The art show drew 3,500 entries, of which 200 were selected for showing at Siggraph and at the San Francisco Museum of Modern Art. Siggraph's industry exhibit will introduce a number of new graphics controllers and displays. A series of technical papers and courses will also be presented. One covers fractals, the self-replicating mathematical form that produces many of the most lifelike computer displays. Bernard Mandelbrot, the pioneer of fractal geometry, will give the course. —Clifford Barney



lite communications ventures involving Hughes Aircraft Co. and rival Ford Aerospace & Communications Corp. Also approved is Teleway Japan Corp., in which Japan's Ministry of Construction has a partial interest. Teleway plans to lay 34 km of optical-fiber cable in the Tokyo subway system and lease the lines to securities firms and banks at rates up to 20% cheaper than NTT's.

The new laws also divide Type 2 carriers into two classes: ordinary, which

service only individual companies or groups, and special, which offer database access to the general public. Close to 100 companies plan to enter the more limited ordinary category.

But it's the Type 2 special class that attracts heavy hitters such as NTT, Hitachi, and Fujitsu as well as joint ventures involving IBM-Japan with Mitsubishi Electric, Marubeni with Tymnet, and GTE Telenet with Intec.

The latest tie-up, an ambitious joining

of forces between AT&T Co. and 16 Japanese partners, was announced earlier this month [*Electronics*, July 8, 1985, p. 11]. Within a few days, General Electric Co. will reveal details of a VAN agreement with NEC Corp., which already has its own domestic network.

Major equipment makers such as Fujitsu, NEC, Hitachi, and IBM see a double payoff. They expect to earn profits on VAN services—though most industry watchers believe it will be two or three

TEXTURES AT SIGGRAPH



years before any operation is in the black—but the big reward they see is sales of personal computers, terminals, modems, and multiplexers used by the networks. A recent report by W.I. Carr, Sons & Co.'s Tokyo office forecasts that demand for integrated systems linked to VANs will grow as much as 40% annually for the next few years.

Because major Japanese companies are trying to cash in wherever possible, the Japan market shapes up as a noodle

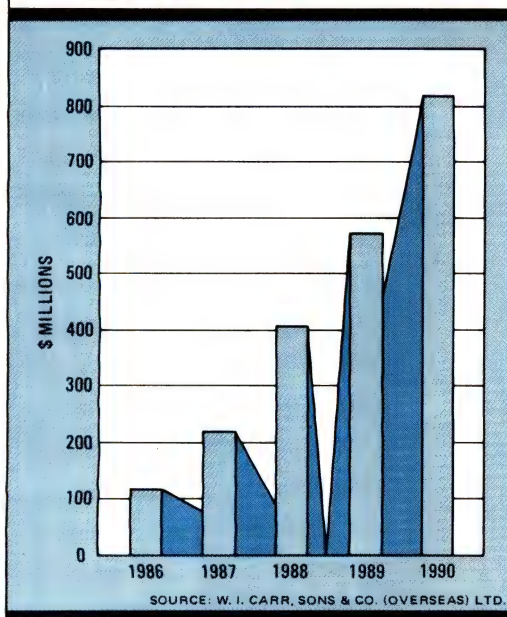
bowl of interlocking relationships. IBM-Japan Ltd., which will begin operating a version of its Information Network system in October, has also set up its own marketing venture in collaboration with Mitsubishi and Cosmo 80 Ltd., a software producer.

Mitsubishi Electric Corp. has a separate arrangement with Teleway, as does Mitsui & Co. Hitachi Ltd., which has its own domestic network, is collaborating with the Marubeni-Tymnet team for in-

ternational access. NEC's new agreement with GE's Information Services Co. (Geisco) lets NEC benefit from GE's IBM interface capability. NEC, which has chosen to go its own way and develop a proprietary operating system, hopes this new IBM compatibility will let it finally penetrate the important U.S. computer market.

The GE agreement also gives NEC entry to GE's Mark III international network, which covers more than 700 cities

JAPANESE VAN MARKET SET FOR GROWTH



in 48 countries. For Geisco, the new venture is a major expansion of its Japanese marketing, which had been handled solely by Dentsu International Ltd.

Fujitsu and Hitachi's equity position in Japan ENS Corp. appears to have given the new AT&T VAN venture a similar international market value. "If Hitachi and Fujitsu hadn't joined the group and made significant technical alter-

tations in AT&T's Network 1000 [a U.S. VAN], Japan ENS wouldn't even have been announced," says the Yankee Group's Japan office director, Stephanie N. Johnson. "They've come up with a system, but it contains so much custom software work that it's not going to look much like Net 1000."

Japan ENS expects to offer packet-switching network services using lines leased from NTT along the Tokyo-Nagoya-Osaka-Kobe corridor by the end of this year. Testing will start in August for international connections to Net 1000 in the U.S., and the plan calls for a fuller array of services including information processing and data storage within the first half of 1986.

Most of the early growth for VANs will be in the domestic market, because current MPT regulations compel networks to use Kokusai Denshin Denwa Corp. for all foreign communications. MPT has announced that it will decontrol this sector by next year. If it does, then the Japanese VAN market will be less regulated than in the U.S. and other nations where CCITT regulations restrict the reselling of VAN services internationally to common carriers.

—Michael Berger

SOLID STATE

BRITISH WAFER-SCALE PROCESSOR MOVES AHEAD

Southampton, England

Researchers at Brunel University are designing a wafer-scale processor they say will perform a remarkable variety of high-performance tasks. The wafer, which will work as an add-on processor to a computer, could have uses in image and speech processing, word and file processing, data-base management, knowledge-base systems, high-resolution-graphics processing, and support of fifth-generation declarative languages.

Funded by Britain's Alvey fifth-generation computer program, Brunel's wafer-scale associative string processor, or WASP for short, will consist of tens of thousands of processors built on a 4-in. wafer using a standard 2.5- μ m CMOS process. The wafer would automatically configure itself to bypass faulty elements and would dissipate about 25 W, says the project's leader, Mike Lea [*ElectronicsWeek*, Feb. 25, 1985, p. 20].

The feasibility study at the Uxbridge university is part of a research program into the design of fault-tolerant chips and wafers. Other participants are The

Plessey Co., General Electric Co. plc, and International Computers Ltd.

Brunel's preliminary conclusions were presented at the International Workshop on Wafer-Scale Integration, held at Southampton University in mid-July. In a series of four papers, Lea and his colleagues concluded that WASP is not only workable but could show a twofold cost advantage over systems built from very large-scale integrated circuits. WASP's associative string-processing architecture uses silicon efficiently and is easily reconfigured to tackle many types of data-processing problems.

Regular structures with short interconnections work best in silicon. The systolic array—a matrix of processors, each performing part of a pipelined task—is one example. It is processor-intensive and excels at signal pro-

cessing. Brunel's associative string processor has these characteristics, but is also memory-intensive. "The architecture can support and manipulate abstract data structures such as sets, strings, queues, stacks, arrays, tables, trees, and directed graphs," says Lea.

Smart memory. Lea's ideas stem from a long-standing interest in associative memories. His team has added extra control and communications logic to each memory location to produce, in effect, a distributed intelligent memory.

In the WASP structure, a communications bus links associative processing elements. Processors compare their register contents with the activity on the bus. When there is a match, they execute a local operation, such as read, write, or add. The array is loaded serially.

The architecture works nicely for both wafer-scale and VLSI implementations. The Brunel team is just completing two special-purpose VLSI circuits. Scape, for single-chip array-processing element, packs 256 image processors onto a chip; first silicon is due this month. Script, for single-chip relational information-processing element, is intended for text-processing applications; it is due out in the first quarter of 1986. Both pack a lot of processing power. Each is an associative memory array with microprogrammed bit-column and word-row control logic. Fault tolerance can be built in by providing spare rows.

Brunel is applying the same architecture to wafer-scale circuits, using chunks of the Scape and Script chips as building blocks. WASP is a 7-by-7 matrix of chip sites, each 1 cm square and formed on a 4-in. wafer. These 49 blocks would be assembled from three basic logic structures: an associative-processing block, a communications block, and a wafer input/output block. Communications blocks form a tree-structured network for routing data packets and con-



Waspish. Mike Lea's team at the UK's Brunel University is developing a wafer-scale associative string processor.

trol signals around the wafer.

The array is self-configuring. At power-up, control circuitry applies test signals to all processors in parallel. Each responds with a test signature, and if it is incorrect, the processor is switched out. Because all memory elements are associatively addressed, the array is not disabled by a few missing processors.

The problems in getting the wafer to

work are still formidable. Yet Brunel can take heart from other developments at the conference. For example, Sinclair Research Ltd. gave a working demonstration of its first wafer-scale memory circuits. But Inmos Ltd.'s Iann Barron warned that "wafer-scale integration has yet to find an application where it can find sufficient advantage to yield a major entry point." —Kevin Smith

TELEVISION STANDARDS

JAPANESE TEAM SETS OUT TO UPGRADE TV IMAGES

Tokyo

Even as NHK, the Japan Broadcasting Corp., continues its singleminded development of a new type of dramatically different high-definition display for future televisions, Japan's government, electronics industry, and commercial broadcasters are taking a more pragmatic approach. They have formed a committee to push ahead with a compatible upgrade of the NTSC 525-line color-broadcast format, used in Japan and the U.S. Proponents of the upgrade hope to have a fully tested system adopted by the end of 1988.

Moving directly to HDTV was never a real option for the government or broadcasters. It would have meant setting up a completely different broadcast system because it would not be compatible with the existing TVs in Japan's 40 million households. In addition, HDTV signals must be transmitted by direct-broadcast satellite. The reason is that the 1,125-line signal needs too much bandwidth for a terrestrial channel, even in the most compressed mode available today [*Electronics*, Feb. 23, 1984, p. 74].

To improve the quality of the picture produced by the 20-in. TVs common in Japan, the group chaired by the Ministry of Posts and Telecommunications will work on both vertical and horizontal resolution. Vertical resolution can be bettered by cameras that produce a noninterlaced scan; horizontal resolution is increased by adding additional horizontal-signal components.

Sets smaller than about 30 in. do not need 1,125-line resolution, says Kiyoshi Iida, deputy director of the Engineering Division of the Broadcast Administration at the MPT. He adds that 30-in. sets are too big for most Japanese houses.

Japan has two basic alternatives to HDTV in the works. Extended-definition TV (EDTV) uses a new type of camera and preprocesses the image before transmission; such systems have been proposed by Asahi Broadcasting Corp., a Japanese TV network in Osaka, and by Hitachi Ltd., Tokyo. Improved-defini-

tion TV (IDTV) seeks an improved picture without new broadcast equipment, using a postprocessor at the receiver.

Today's TV systems use an interlaced scan in which alternate lines of a TV frame are scanned on the first field of a frame and the remaining lines on the second field. In the NTSC system, 262.5 lines are scanned during the 1/60-s period of each field, for a total of 525 lines during the 1/30-s period of each frame. This scheme was necessary to achieve current picture quality in the analog era, but it provides only about 60% to 70% of the vertical resolution possible with a noninterlaced display with the same number of lines.

Asahi's and Hitachi's EDTV systems incorporate a camera with noninterlaced scan, a frame memory at the camera for transmission of alternate fields compatible with NTSC TV, and a frame memory in the TV to reconstitute a noninterlaced display. Both use preprocessing at the camera, which simplifies the task of re-

constituting the frame in the TV set.

Though the systems are similar, the two groups disagree on details. Hitachi's IDTV system synthesizes noninterlaced frames at the TV using many of the same techniques needed for EDTV, including memory. NEC Corp. and others are also starting similar work. In fact, virtually all Japanese TV makers are working on IDTV based on the development of digital TV improvements. Some are extremely bullish on EDTV and IDTV, and a number of engineers predict that future demand for frame memory in TV and video cassette recorders will far exceed that for computer memory.

Empirical. Asahi's EDTV system starts with a modified TV camera designed for one noninterlaced frame every 1/30 s. It incorporates a 0.73-megabyte one-frame memory to store complete frames and to transmit alternate NTSC-type fields. The system requires a 1.47-megabyte two-frame memory in the receiver. Hiroshi Shibata, who developed the system, says the 1/30-s frame period eliminates motion between a frame's

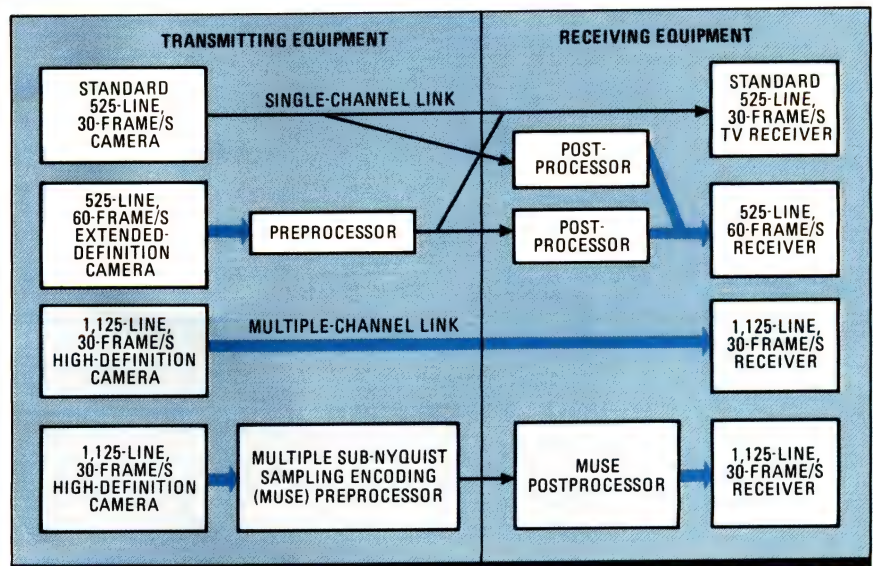
two fields, so reconstituting the frame in the receiver is simple.

Critics of the system note that pairs of successive frames displayed by the TV are

identical, which can give rise to jerkiness. Shibata says pictures appear to have natural motion, and he points out that movies use a similar scheme with the lower frame rate of 1/24 s. Another criticism is that the moving objects become blurred during the 1/30-s exposure of each frame. But Shibata says that cutting exposure time with a shutter gives rise to unnatural effects.

Hitachi bases its systems on three-

High-definition TV proposal is too ambitious



TV maze. The Japanese are exploring possibilities for improving TV pictures (top half) without resorting to approaches incompatible with current sets and channel allocations (bottom half).

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dimensional frequency-domain analysis of the signal. Older design methods no longer suffice, says Takahiko Fukinuki, a chief researcher at Hitachi's Central Research Laboratory, who heads the EDTV group. The research shows that a vacant space remains in the transmitted frequency spectrum despite the addition of the color subcarrier.

The broadcast signal has two luminance-signal components for each color-signal component, providing space for another signal in the same frequency range as the color subcarrier. Hitachi wants to use this space to extend the horizontal resolution. Three-dimensional frequency-domain filters, which use frame memories to add time to the equation, are best for separating luminance, color, and extended-horizontal-signal components.

Frame buffers may use vast amounts of RAM

Hitachi starts out with a camera designed for one noninterlaced field every 1/60 s. Preprocessing before transmission includes storage in frame memory, filtering to remove signal components that cause aliasing, and insertion of high-frequency components.

The receiver recovers color and enhanced horizontal-resolution components and interpolates missing scan lines using motion-adaptive filters. Critics say that rapid motion appears unnatural, which indicates that the Hitachi systems have not yet been perfected. But their customers must think the company is on the right track: Hitachi has limited but steady sales of an expensive IDTV adapter for computer-aided instruction and large-screen projection systems for theaters.

—Charles L. Cohen

Pewaukee, Wis. Tests of video and other broadband applications will be conducted between two printing-plant sites about seven miles apart.

"In the industry, there have been a number of experiments and developments over the past five to six years, but [fiber-optic links to subscriber sites] have not been deployed on a large scale," notes Neven Karlovac, director of lightwave product development at the Collins division.

Wisconsin Bell—one of five midwestern Bell operating companies owned by American Information Technology Corp. of Chicago—will pass the lightwave signals through its central-office switches and will be studying possible network applications during the trials.

During the tests, near-infrared signals—with wavelengths of 1.3 μm —will carry data at 44.7 and 139 Mb/s. Initially, Rockwell will use commercially available light-emitting diodes and detectors. But the company is developing its own technology based on indium-phosphide-based 1.3- μm edge-emitting LEDs and detectors tightly coupled to 8- μm single-mode fiber to minimize signal loss.

High-loss fiber. Rockwell's plan is to have lightwave signals travel as far as 73 km without repeaters. Such long-distance capabilities can translate into lower costs for short local telephone-loop networks—so higher-loss fiber can replace more expensive low-loss cable, for example.

Price is crucial to the spread of fiber optics, and it is falling fast, according to Electronicast's prediction. Since 1980, the price of fiber-optic communications systems, in dollars per megabit kilometer, has dropped more than two orders of magnitude.

The fibers now sell for \$450 per fiber kilometer. Dixon estimates that by 2000 this price will drop to \$140. He says, "That is close to the cost of simple copper wire, and yet fiber can handle thousands of times the data without being amplified."

At the same time, Dixon points out, "A great deal of progress is also occurring in the circuit area. Eventually the industry will get into integrated optical circuits."

Vapor-phase epitaxial deposition of thin layers in indium gallium arsenide phosphide compounds also promises to cut the cost of materials for 1.3- μm lasers and LEDs. Dixon observes, "Today, the cost of long-wavelength lasers is \$1,000 to \$1,500, even in volume. We see those prices dropping to a couple of hundred dollars." —J. Robert Lineback

LIGHTWAVE COMMUNICATIONS

LOCAL LOOPS MAY BE NEXT FIBER-OPTIC MARKET

Richardson, Texas

Fiber-optic systems have so far been tried out mostly for long-haul trunks. But fiber optics' true long-term potential may lie in local subscriber loops. "Ten years from now, the biggest market will be local distribution," says Frank W. Dixon, president of Electronicast Corp. of Redwood, Calif.

Electronicast, which does consulting work in the lightwave-communications field and last month hosted a seminar on lightwave-technology trends in the year 2000, estimates that this year worldwide revenues from lightwave-component sales to telecommunications markets will total \$1.34 billion.

That figure is expected to approach \$40 billion in 15 years (see chart). During that period, local telephone networks will come to account for the majority of fiber-optic telecommunications transmissions.

Some U.S. metropolitan telephone operating companies have run fiber cable directly to large corporations, but as volumes grow, Electronicast's Dixon expects lightwave to open up broadband applications even in the home.

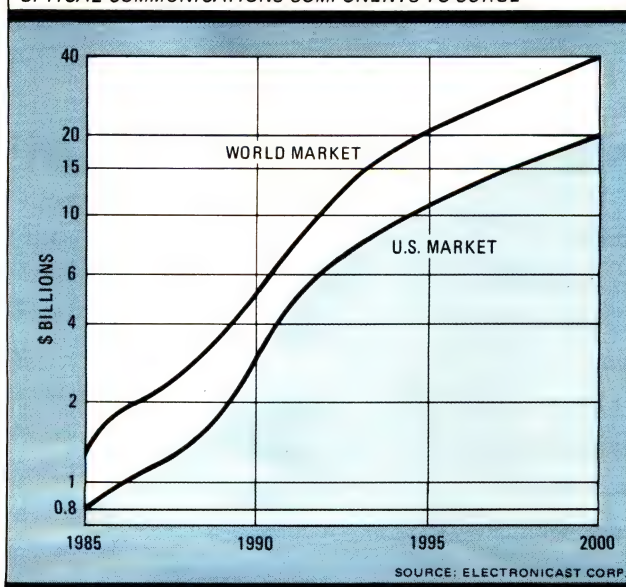
"Video applications will be one of the early applications to help defray the cost. High-resolution digital television will also figure in, with digital transmission requirements be-

ing 80 to 90 Mb/s," predicts Dixon.

Already, hardware makers and telephone operating companies are readying themselves to tap that potential. Major contenders in the field include AT&T Communications, L.M. Ericsson, Fujitsu, NEC, Northern Telecom, Plessey, and Teleco Systems.

Rockwell International's Collins Transmission Systems Division in this Dallas suburb intends to join that group. Trials of Rockwell's subscriber-loop lightwave-communications equipment will start in September at Quad/Graphics Inc., a printing company in

OPTICAL COMMUNICATIONS COMPONENTS TO SURGE



LASER IS STAR, THANKS TO STRIPES

Munich

Designers working on certain semiconductor-laser applications may soon have the power for which they've yearned. Optoelectronic specialists at Siemens AG's Central Research Laboratories are coming through with laser arrays that integrate 10 or more laser stripes on a single chip.

The lab has readied a prototype gallium-aluminum arsenide laser chip that integrates 12 light-emitting regions (stripes). This boosts the array's output to 300 mW continuous wave for each of its two light-emitting surfaces, or facets, and its power-conversion efficiency as high as 30%.

Having already perfected long-life single-stripe lasers that have high stability, the Siemens researchers think that these arrays, with between 10 and 40 optically coupled laser stripes per chip, are the next logical step. The company has carved out a sizable chunk—between 30% and 40%—of Europe's market for 880-nm semiconductor lasers.

The maximum output from a single-stripe semiconductor laser, by contrast, is typically 50 mW cw for commonly used structures and 100 mW cw for special structures, according to Franz Kappeler, head of the laser-array development team at the research labs. These limits restrict such devices to jobs in communications as well as in video and audio playback systems. For tasks that demand higher power levels, equipment designers had to turn to such bulky and inefficient alternative sources as gas lasers.

The laser array's high power, coupled with good coherence properties and small size, opens up a wide range of applications to semiconductor lasers. Arrays could be used as pumping devices for neodymium yttrium-aluminum-garnet lasers and for direct triggering of high-power optically ignited thyristors, for example.

Blue light. Spectroscopy offers another interesting application. A laser array can be used to halve the wavelength (double the frequency) of light in nonlinear crystals to obtain, for example, a coherent source of blue light. Furthermore, if several arrays are arranged side by side in the form of an array bar, they can be used as a line source (instead of a point source) for applications such as infrared illuminators in military night-vision systems. Medical equipment could also use laser arrays.

The 12-stripe Siemens array, which radiates light at wavelengths ranging from 805 to 880 nm, may be available as samples from the company's Munich-based Components Group late this year, according to Kappeler.

Even better results have been obtained with arrays that are still in the experimental stage. A 40-stripe array, also of GaAlAs, gets up to 1.65 W cw per facet and boasts an efficiency of better than 33%. It emits light at 880

nm structure (the type used for the 12-stripe prototype array) or the more recently developed multiple-quantum-well (MQW) structure (used in the 10- and 40-stripe experimental versions).

As Siemens fabricates the MQW structure, the active layer consists of four potential wells, each separated by a potential barrier. In this type of structure, the recombination of the charge carriers generally takes place only between a very limited number of energy levels in the conduction and valence bands. This reduces optical losses in the laser material and enhances the laser's efficiency.

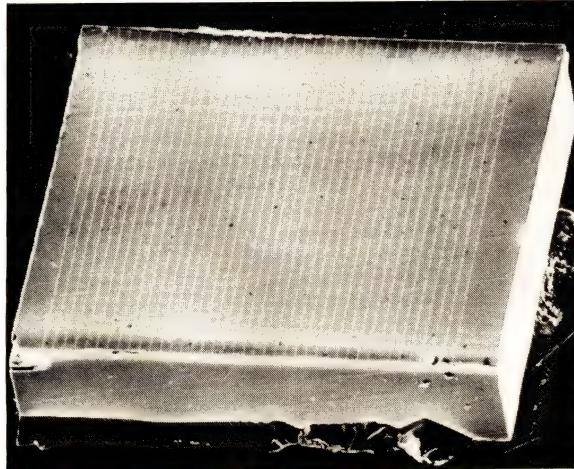
The Siemens array, with its multiple GaAlAs layers on a gallium arsenide substrate, comes as a chip that measures 0.4 by 0.5 mm and 100 μ m thick. The stripes are about 400 μ m long and 3 μ m wide. The center-to-center spacing is typically 10 μ m (see photo). The array emits power in two lobes within 7° of each other; each lobe is less than 2° wide. This sharp bundling results from the phase-locked operation of the array emitters.

Several factors combine to produce the 36% efficiency that Kappeler says "is by far the best value reported until now." Foremost is the low electrical series resistance—0.1 Ω —for the 40-stripe laser.

This low figure results from the extreme homogeneity of the epitaxial layers, which Siemens has obtained with an optimized MOVPE process and a sophisticated contact technology that was developed in-house. The efficiency of the experimental laser arrays is up to two times higher than that of competitive devices.

Also contributing to high efficiency are a low threshold current (22 mA per stripe) and a good slope efficiency (0.55 W/A per facet). A 1- μ s pulse test of 10 double-heterostructured arrays evenly distributed over a 14-mm bar showed that all arrays put out a uniform 0.75 W per facet at 807 nm with less than a 5% deviation for both the threshold current and the slope efficiency.

As a result, a 1-cm-long bar that contains about 70 arrays can produce an output of at least 50 W for 1 μ s at a repetition rate of up to 10 kHz. The high uniformity of the device parameters across the whole wafer demonstrates that semiconductor laser arrays grown by MOVPE can be fabricated with high reproducibility on a production-line scale, Kappeler points out. —John Gosch



Power lines. Siemens' experimental semiconductor laser array has 40 stripes, each 400 μ m long and 3 μ m wide.

nm. Another experimental device, a 10-striper of the same material and wavelength, checks in at a 36% efficiency and a per-facet output of 0.86 W cw.

Siemens is not the only company active in semiconductor laser arrays. In Japan, both the Tokyo Institute of Technology and Tohoku University have built experimental arrays [*Electronics Week*, June 3, 1985, p. 30]. Already on the market in the U.S. with a laser ar-

Optically coupled stripes multiply output of semiconductor laser

ray is Spectra Diode Laboratories Inc. of San Jose, Calif., a joint venture of Xerox Corp. and Spectra-Physics Inc., San Jose. However, Kappeler thinks his firm has the leg up on the competition in terms of efficiency and output power.

To fabricate the arrays, Siemens and the U.S. firm use metal-organic vapor-phase epitaxy (MOVPE), a process that makes for thinner and more homogeneous layers than does the familiar liquid-phase-epitaxy technique. The MOVPE process produces wafers with either a conventional double hetero-

THE GAME COULD BE OVER IN JAPAN MARKET FOR U.S. CHIP-EQUIPMENT MAKERS

by Michael Berger

AMERICANS FIGHT TO HOLD 25% OF BUSINESS THEY ONCE OWNED AS JAPANESE COMPETITORS GEAR UP FOR U.S. MARKET

Tokyo

Ten years ago, the future looked great for U.S. makers of chip-production equipment in Japan. In 1975, close to 80% of all production equipment purchased by Japanese companies bore the stamp "Made in U.S.A."

This year, in a market valued at close to \$3 billion, the numbers have almost reversed. Nearly 75% of semiconductor-production equipment sales in Japan will be made either by Japanese companies or Japan-based joint ventures with U.S. makers (see table).

The dramatic turnaround is evident in nearly every area of the industry:

- In lithography, a Japanese market that will be worth more than \$500 million in 1986, Canon Inc. controls 90% of contact-aligner sales and has seized 40% of Perkin-Elmer Corp.'s virtual monopoly in projection aligners.

- In dry-etching equipment, estimated to be worth more than \$150 million next year, Anelva Corp., an NEC Corp. subsidiary, has overtaken world market leader Applied Materials Inc.

- In film deposition, Anelva also leads in Japan's \$67 million sputtering-equipment market and has a Silicon Valley assembly base in San Jose, Calif. In epitaxial chemical-vapor deposition (CVD), Kokusai Electric Co. has pulled even with Applied Materials and is pushing a joint venture between Tokyo Electron Corp. and Thermco Inc. in low-pressure CVD.

On to America. Industry analysts predict that within the next five years Japanese companies in all market segments will have established manufacturing bases in the U.S. Nikon, which took away two of GCA Corp.'s largest Japanese clients—Toshiba Corp. and NEC—is already pursuing the leading U.S. chip makers. Motorola Inc., for example, has shown interest in Nikon's stepper equipment.

Canon has opened general sales offices in New York, Dallas, and Santa Clara, Calif., for its aligner equipment, plus offices in Houston and

Lubbock, Texas, where Texas Instruments Inc. has manufacturing facilities. Ulvac Corp., Tokyo, reportedly has sold a number of sputtering systems to IBM Corp.

The strategic response to yet another Japanese challenge seems clear. "To succeed in Japan, you must experience this market in all aspects, including manufacture," says Tetsuo Iwasaki, president of Applied Materials Japan Inc. Formed six years ago, the company has seven offices in Japan, including a technology center that opened last October. The ultimate goal is full manufacturing.

The lower cost of capital in Japan poses another disadvantage for U.S. companies. Thus many have chosen a less expensive route—joint ventures with Japanese partners. Tokyo Electron Corp. is the standout example, having made 50-50 joint ventures with the likes of Varian Associates Inc. (ion implanters), Thermco Inc. (diffusion furnaces and plasma CVD systems), and Lam Research Corp. (dry-etching equipment).

This strategy has enabled the U.S. makers to hold their market share and increase sales, but joint ventures do not work if a company wants access to new technology, say some critics. The Japanese partner usually is interested only in sales. That's what happened at Applied Materials, which ended its relationship with Kane-matsu Semiconductor Corp.

Even GCA, faced with the Nikon challenge, had to realign its long-time relationship with Sumitomo Corp. Two years ago, GCA formed a new company with its old agent, built a testing and assembly plant, set up a new distribution system, hired Japanese engineers, and began to purchase subassembly equipment from Japanese vendors with the goal of manufacturing entire systems. GCA's immediate goals have been met, says Donald

Presence. Applied Materials Japan has seven offices, including this technology center.

Baumann, Far East director. "We've stopped losing market share, and we're set to regain some." But market analysts are skeptical about whether the Americans can do more than hold the line.

"The key is not the established customers, but the newcomers," says Shiro Tanikawa, a researcher in the electronics industries section at the Nomura Research Institute, Kamakura. "I think Nikon, being a Japanese company, will be more effective in getting the business of the newcomer firms. GCA may maintain its Japan market share, but Nikon is going to gain world market share."

Outlook unclear. Because the semiconductor slump shows no signs of turning around, the immediate market outlook for all players is not a bright one. Tanikawa sees a possible upturn by next spring but warns that on the end-user side the office-automation market in Japan has been sluggish. Analyst Peter Wolff of Prudential-Bache's Far East Research office in



Tokyo is a bit more bullish. "The semiconductor companies have reduced capital spending, but most of that is new land purchases. The plants already planned or under way are going ahead, so new equipment still will be installed."

Regardless of when the market does take off again, the U.S. makers face a number of serious problems. One of them is in Washington. Defense Department export restrictions have delayed shipments to Japanese customers, and in a fiercely competitive market such as Japan, the U.S. cannot afford another barrier.

Two other problems crop up when companies do business in Japan. The first is that it is difficult to recruit in an industry that generally practices lifetime employment.

Customer rules. But the ultimate problem is that the market has developed, as Japanese markets usually do, into a struggle between companies with comparable technology to see which can serve the customer best. "There has been an automation boom in semiconductor production," says Shigeru Nakayama of the Tokyo office of the U.S. Semiconductor Equipment and Materials Institute. "If the U.S. makers don't pay attention to this trend and work even more closely with customers, the Japanese will develop a major advantage."

As if that weren't enough, another challenge is on the way. The Ministry of International Trade and Industry is organizing an eight-year program to develop the next generation of production technology and is seeking \$120 million for the program, which could begin next spring. □



A FEW COMPANIES DOMINATE IC-EQUIPMENT MARKET IN JAPAN

Process		Projected 1986 Market (\$ million)	1984 Market Share (Value basis)	
LITHOGRAPHY				
Mask generation	Electron-beam	48	Nihon Denshi Co.	45%
			Perkin-Elmer Corp.	20
			Toshiba Kikai Co.	20
Photolithography	Other	8		
	Contact Aligners	12	Canon Inc.	90
	Projection Aligners	56	Canon	60
			Perkin-Elmer	40
	Steppers	320	Nikon Inc.	60
			GCA Corp.	35
			Optimetrix	5
Spinners		100		
Total Lithography		544		
ETCHING				
Dry etching	Plasma Etching	52	Tokyo Ohka Industrial Co.	35
			Tokuda Seisakisho Co.	25
			Branson /IPC	15
Ion Etching		100	NEC Anelva Co.	65
			Applied Materials	20
Wet Etching		4.8	Dainippon Screen Mfg. Co.	40
			Kaijo Electric Co.	30
Total Etching		157		
DEPOSITION				
Chemical-vapor- deposition equipment	Normal Pressure	18		
	Low Pressure	62	TEL/Thermco Co.	45
			Kokusai Electric Co. Ltd.	40
	Plasma	28		
Epitaxial		60	Applied Materials Inc.	35
			Kokusai Electric	35
			JPC Electronics Corp.	10
Plasma-vapor- deposition equipment	Vacuum Evaporator	26	Ulvac Corp.	50
			NEC Anelva	25
Sputtering Equipment		67	NEC Anelva	30
			Varian	30
			Perkin-Elmer	10
			Ulvac	10
Total Deposition		260		
ION IMPLANTATION				
Ion implanters	Medium Current	40	TEL/Varian Co.	45
			Ulvac	45
High Current		84	TEL/Varian	45
			Eaton-Nova	45
Annealing		4		
Diffusion/Oxidation Furnaces		36	TEL/Thermco	80
			Kokusai Electric	15
Total Implantation		164		
SOURCE: NOMURA RESEARCH INSTITUTE				

SOURCE: NOMURA RESEARCH INSTITUTE

IN HARD TIMES, VENTURE CAPITAL TAKES ON NEW ROLE

by Larry Waller

PHOENIX VENTURES, LED BY TOP 'COMPANY DOCTOR,' TAKES CONTROL OF FINANCIALLY AILING HIGH-TECH FIRMS

Los Angeles

Venture capitalists sank billions of dollars into hundreds of new electronics companies during the startup frenzy of the early 1980s. But now, as the market turns sour and with a turnaround somewhere in the uncharted future, they have all but put an end to that activity. The question before them is what part to play in high-tech entrepreneurship in troubled times.

To one investment bank, these widespread woes signal heightened opportunity. San Francisco's Hambrecht & Quist Inc., noted during the past decade for snapping up troubled companies and turning them into winners, has added a new twist to turnarounds. The bank created a \$32 million fund to buy control of firms that are strapped for cash but otherwise look to have solid potential.

For now, it is the only such turnaround venture in operation, though others in the business are thinking of similar enterprises. One who decided against it is Richard Kramlich of New Enterprise Associates, a San Francisco venture-capital firm with \$200 million in its kitty. Some troubled companies can be had for as little as 5c on the dollar, he says, which further whets capitalist appetites. But, adds Kramlich, the investor needs a management team to run the companies, "which Phoenix has and we haven't."

Foreign sources. The Hambrecht & Quist fund, called Phoenix Ventures, was organized as early as 1983 when H&Q began raising the money (eventually all of it) from foreign investors, and announced officially that it was open for business in September 1984. But it actually made its first investments before that: in Diasonics Inc., Milpitas, Calif., in April, and in Adac Laboratories, San Jose, Calif., in August. This year, it took on Rexon Inc., Culver City, Calif., in January and Miniscribe Corp., Longmont, Colo., in May.

The H&Q turnaround approach always features hands-on management, largely supplied by chairman Q.T. Wiles,



Offers relief. Q.T. Wiles has a cure for ailing companies.

who has forged a reputation as the foremost "company doctor" in the industry. Wiles serves as chairman of three Phoenix Venture firms and with his staff of about a dozen executives, actively oversees their affairs from his Bay Area office. (But because Adac and Diasonics both manufacture medical diagnostic equipment and are potential competitors, another H&Q official, Stewart Carrell, was selected to run Diasonics.)

'We don't get our opportunity until things are bad'

Wiles recalls that the idea for Phoenix Ventures rose from talks he had with H&Q's chief executive officer, William Hambrecht, in June 1983, at the peak of the technology boom. The two investment veterans suspected that a business slide was in the offing, as the inevitable reaction to speculative excesses. "It was apparent then that companies would need some help to come out the other

side," Wiles explains.

Events unfolded as foreseen, and now "a whole lot of good companies out there need money but can't get it," he observes. Though H&Q officials try to identify companies in advance for possible investment, opportunities often pop up unexpectedly and decisions must be made quickly. Quips Wiles, "We are the last resort, and make the deal the day before bankruptcy."

Phoenix Ventures general partner Daniel Case confirms this timing: "We don't get our opportunity until things are bad." But

he points out that as long as the target investment has only a cash problem, buying an existing company is preferable to starting a new one. "The real advantage is that there is something there to fix, instead of creating it out of thin air."

Reconstruction. Wiles does not downplay how tough righting any failing enterprise can be. For starters, "management has to be restructured in almost every instance," he says. His vigorous housecleaning at acquired firms have entered the turnaround lexicon: the verb "to Q.T.-ize" describes the approach he takes.

But when executives of proven competence are already on hand, Wiles says that he is happy to let them continue and to support them. "That's the toughest part—getting the right people. The ones I know elsewhere who can do the job are too smart to take it."

Furthermore, changes cannot proceed too fast, since it takes the H&Q group "a quarter to have some understanding of what goes on, and another quarter to find out where all the bodies are bur-

ied," Wiles explains. One puzzler is figuring out where a firm's products stand in relation to the competition, a job compounded by onrushing technological developments.

This is particularly tough in the computer-peripheral business, which H&Q is entering this year with two partners: drive-manufacturer Miniscribe and Wangtek, a subsidiary of REXON and manufacturer of backup 1/4-in.-tape drives.

In reorganizing a troubled company, the H&Q approach initially eschews infusions of technology. Instead, it sticks with basic business techniques, installing tight reporting systems and finan-

Phoenix's formula always involves a hands-on approach

cial controls and generally instilling discipline in management. In most cases, these were lacking in companies that were too technology oriented to pay attention to the fundamentals of running a business.

"I know we [at Wangtek] didn't have them," says Whitney G. Lynn, vice president for marketing at the Simi Valley, Calif., company. He notes that Wiles and his staff moved quickly to make these changes, which closely track cash flow and improve planning.

Cash available. The H&Q turnaround venture has not escaped the attention of the financial community, where venture capital firms still have plenty of cash on hand—some estimate as much as \$500 million—but a scarcity of solid new ideas in which to invest. "A lot of the really good opportunities right now are in saving companies," notes Michael Murphy of Venture Capital Management Inc., in San Francisco, and publisher of the "California Technology Stock" newsletter.

But the pitfalls are obvious, cautions Case. "Many venture capital firms don't have the special skills for it." New Enterprise's Kramlich agrees. "You need a commando squad that knows what it's doing."

Another question concerns payoff, or, in Kramlich's words, "What's the upside?" Even Wiles, whose big winner was Granger Associates Inc., a once-troubled communications firm that was sold last year in a stock deal to Digital Switch Corp. for \$358 million—a profit estimated at \$25 million—doesn't know the answer. "I don't see the end of this story, from where I sit," he says. Meanwhile, H&Q will keep increasing Phoenix Ventures' stake, to a limit of 10 companies, with no single investment of more than 10% of the total fund. □



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Real-Time Operating Systems

Computers which depend on real-time operating systems run telecommunications and data communications, factory automation and process control, the military, and avionics. These operating systems are software programs which allow computers to handle large amounts of data and to respond in "real time"—immediately. New and established companies

are developing the newest generation of these operating systems for personal and engineering computers, as well as newer mainframes and superminis.

Target Readers

Software design engineers, system analysts and designers, technical managers, system integrators, applications program writers, and any users of real-time systems.

Issue Date:
August 19, 1985

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July 29, 1985



Electronics
Influence Beyond Design

A FRENCH PROPOSAL COULD INVIGORATE EUROPE'S HIGH-TECH RESEARCH

by Robert T. Gallagher

A PLAN TO VAULT ITS TECHNOLOGY TO U.S. AND JAPANESE LEVELS IS SEEN AS AN ALTERNATIVE TO PARTICIPATING IN STAR WARS

Paris

The ailing European electronics industry may find the solution to its technological and morale problems in a new French program called Eureka. This alternative to the U.S. Strategic Defense Initiative program (Stars Wars) is a broad-range research and development plan meant to catapult European technology to the level reached by the U.S. and Japan.

Eureka—a program by and for Europeans—was first mentioned confidentially to other European governments in late April by the government of President François Mitterrand. The plan found widespread acceptance from the beginning, even before there were enough proposals on the table for anyone to know what direction the plan might finally take.

The first official gathering aimed at defining Eureka, held in Paris last week, took the form of an ad hoc meeting for research ministers of those European countries that would like to participate in the plan.

Chaired by Hubert Curien, France's minister of research and technology, the meeting confirmed its support of a detailed French proposal that was formulated in consultation with other European governments and industries. It also backed a West German initiative supporting research in supercomputers, particle accelerators, waste disposal, and biotechnology, and a British white paper proposing an initiative called Eurotype, a kind of "buy European" act for high technology.

The French proposal calls for the adoption of five general programs, three of which fall within the broad category of electronics: Euromatique, for data-processing systems and components; Eurobot, for

robotics and industrial automation; and Eurocom, for telecommunications and networking (see chart). The remaining two programs are for research in biotechnology and industrial materials. Nominations to participate in Eureka under the French proposal include virtually every major European electronics company and public research laboratory as well as scores of smaller concerns.

Limited resources. Eureka's significance stretches from Stockholm to Washington. The U.S. government is certain to be watching closely because most European electronics industry executives and government officials do not believe that Eureka and SDI will be able to coexist in Europe. These observers expect the two initiatives will end up competing for limited European research resources. This may pose serious problems for U.S. military planners who, for reasons of both strategy and public relations, have sought European

participation in their SDI program.

At last spring's economic summit in Bonn, attended by President Reagan and other heads of state, U.S. officials were generally noncommittal on Eureka. However, they did say there is no reason that U.S. contractors for SDI could not take on European associates.

Financing is still unclear. Though last week's meeting decided on no firm plans for apportioning the program's expenses, the French government proposed to contribute about \$120 million. Additional finance will come from the other European governments, with the UK and West Germany bearing the lion's share of the burden. Participating organizations and companies will also contribute to their own projects.

Yet another issue to be addressed by the governments involved is just how the complex program will be administered. The consensus at the meeting was to avoid creating an administrative

structure and to leave the coordination of the program firmly in the hands of the industrialists.

Although the European Communities pushed hard to take the program under the umbrella of its European Technology Community (a body recently proposed to coordinate European research), both Mitterrand and British Prime Minister Margaret Thatcher balked, announcing publicly that they didn't want Eureka mired in the EC bureaucracy.

Still, the first cooperation contracts were signed weeks before concrete proposals for either an administrative organization or financing for the program had even been considered. France's Matra SA and Norway's Norsk Data will jointly develop compact vectorial computers; the UK's General Electric Co. plc, NV Philips of the Netherlands, Siemens AG of West Germany,

EUREKA CONCENTRATES IN THREE AREAS

EUROMATIQUE

- Large vectorial computer
- Highly parallel computer architectures
- Multiprocessor synchronous-architecture machines
- Mass memory
- Software-engineering center
- Symbolic machines
- General tools for expert-system applications
- Multilingual information system
- Management and supervision of industrial processes
- New-generation microprocessor
- 64-Mb dynamic RAM
- Gallium arsenide circuit workshop

EUROBOT

- Agricultural robots
- Civil-security robots
- Factory automation
- High-power industrial lasers: carbon dioxide, carbon oxide, ultraviolet, and free-electron lasers

EUROCOM

- Data-processing network for research applications
- High-capacity digital switch
- Wideband communication between data-processing and office-automation systems
- Broadband transmission

SOURCE: FRENCH MINISTRY OF RESEARCH AND TECHNOLOGY

Starter. France's Hubert Curien chaired the first Eureka meeting of European research ministers.

and France's Thomson SA will work together on future generations of integrated circuits.

European Commission president Jacques Delors admits that Eureka is going forward on its own without the administrative role for the commission that he had hoped for. Yet he emphasizes that the commission "must not be disappointed or irritated." Instead, he says, "let's wait to see what kind of wall these masons build," referring to the ad hoc committee of European research ministers. He stressed the need to link technology policy to commercial and trade policy in Europe.

Delors believes Europe's effort to catch up with the U.S. and Japan in technology is a battle to be fought at the negotiating table as well as in the laboratory. He believes that "we must negotiate technology transfers with both Japan and the U.S. The way things stand, they can attract our technology, but we have no access to theirs."

The U.S. government says that allowing European companies to participate in its SDI program is one way to give them access to U.S. technological advances. But in Europe, the U.S. program has met with reactions ranging from unconditional welcome to total dismissal.

Although a number of European companies already have been sounded out about participating in SDI, opinions vary as to what degree the U.S. program and Eureka will compete. What's more, no European government has yet given the go-ahead for its industries to participate in SDI; given the military nature of the program, their approval is obligatory.

In the UK, a number of academics have rejected SDI outright. They formed a committee and addressed an open letter to Vice President George Bush during his recent visit to Europe, saying that SDI makes demands on computer technology that "can never be met." They also wrote that such a system "cannot be designed and cannot be built."

Inevitable competition. Officials at the West German Ministry for Research and Technology believe that the two programs can coexist, but that competition between them will be inevitable. Siemens, West Germany's largest electronics company, considers participation in SDI politically sensitive and is waiting for the Bonn government to decide



whether to allow participation. According to the ministry, no West German company has yet received a firm offer to join an SDI project.

Industry sources in France say that both of the country's largest defense contractors, Thomson and Matra, have been asked to submit proposals to do SDI research. Matra chief executive officer Jean-Luc Lagardère has publicly stated his desire to participate in both programs, subject to French government approval. French government officials, however, decline to comment on whether or not such approval will be forthcoming.

Despite competition with SDI, there is near unanimity on just what ultimately should be used as the benchmark of Eureka's success. With the EC's Esprit fifth-generation-computer program already concentrating on precompetitive, or basic, research, government officials and electronics industry executives across the continent have high hopes that Eureka will take European cooperation one step further—into the arena of product development.

According to Robb W. Wilmot, chairman of Britain's International Computers Limited plc, what Europe does not need at this juncture is more precompetitive research. "Even though Esprit is making a considerable contribution, it is not sufficient for success," he asserts. "We hope that precompetitive research will solve the problem, but Europe has always had a formidable position in precompetitive research—it is the other 99% of the problem that has kept us from success." □

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Real-Time Operating Systems

Computers which depend on real-time operating systems run telecommunications and data communications, factory automation and process control, the military, and avionics. These operating systems are software programs which allow computers to handle large amounts of data and to respond in "real time"—immediately. New and established companies are developing the newest generation of

these operating systems for personal and engineering computers, as well as newer mainframes and superminis.

Target Readers

Software design engineers, system analysts and designers, technical managers, system integrators, applications program writers, and any users of real-time systems.

Issue Date: August 19, 1985

Closing for Advertising: July 29, 1985



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Electronics August 26 issue

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Digital Signal Processing

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Target Readers

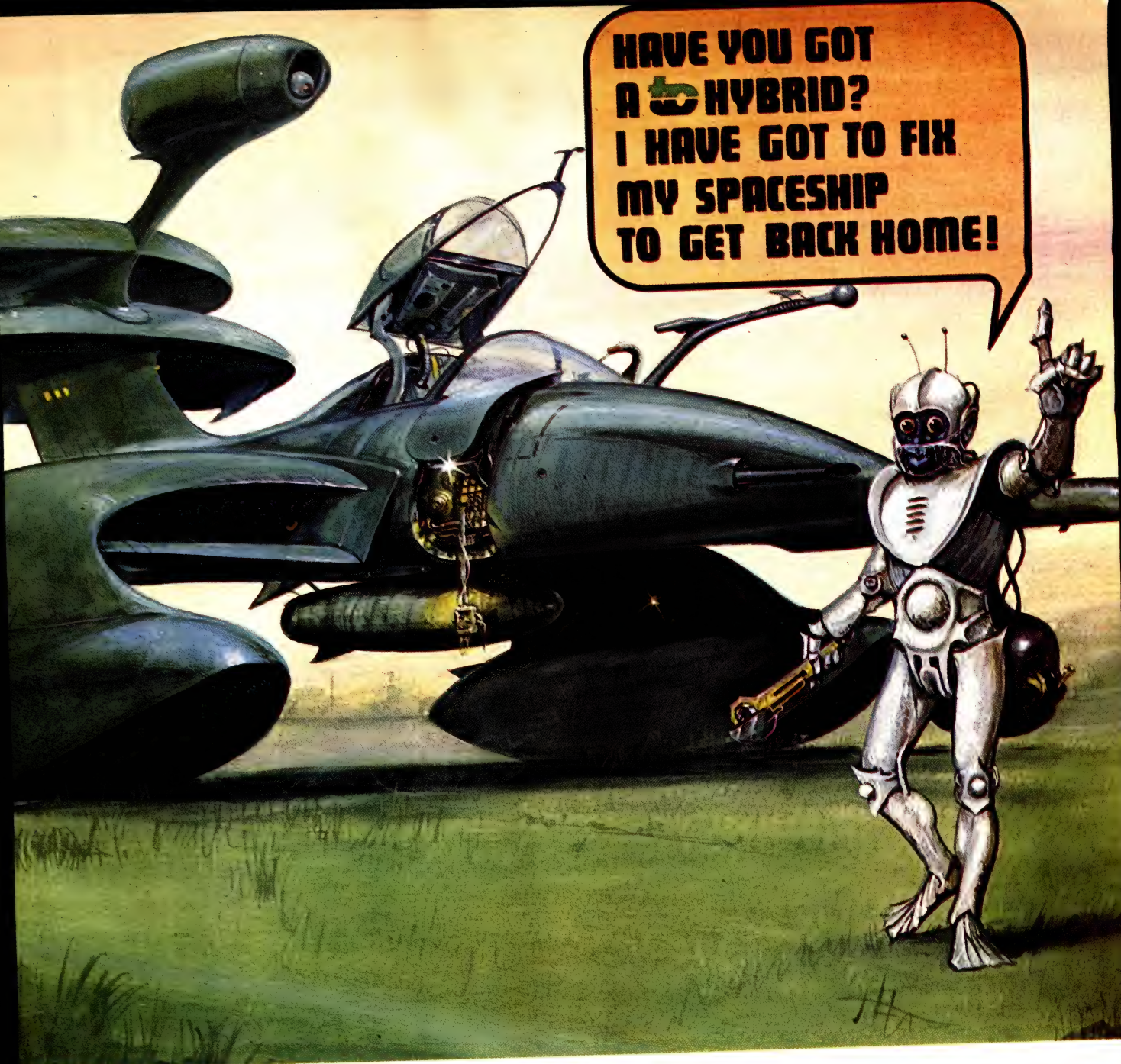
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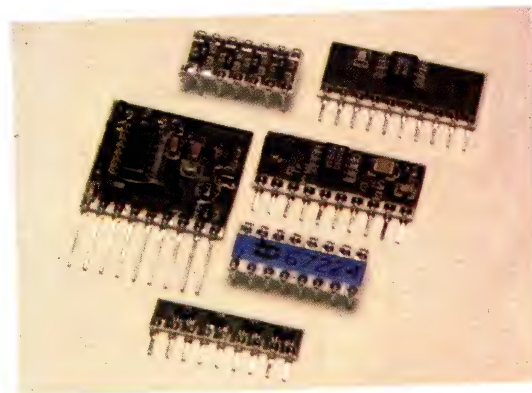
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NEC's NEDIPS—NEC Data-Flow Image Processing System—the world's first practical non-Von Neumann computer is performing well at a remote sensing technology institute in Tokyo.

NEDIPS was originally developed for processing image data from satellite-borne synthetic aperture radar. It has reduced processing

time to about 3 hours from over 100 hours required by conventional mainframes.

Our data-flow computer features three advantages over sequential processing. First, system performance is virtually unlimited by memory input/output speed. Instructions are executed in parallel automatically. Programming and debugging

are easy because it adopts a functional language.

NEDIPS, with a minicomputer like NEC's MS serving as a host computer, consists of an efficient data-flow processor and memory subsystem which is expandable to 64 Mbytes. Maximum processing speed is 159 MFLOPS. Superior speed and programming ease make the system highly suitable for diverse scientific calculations such as dynamics simulation and differential equations, signal processing and general image processing.

NUMBER 133

V20/V30 FEATURE EXTENSIVE CMOS PERIPHERALS.

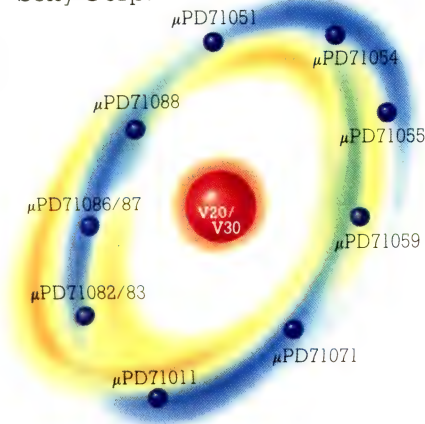
The first 16-bit members of NEC's V-Series CMOS micro-processor family are available with CMOS peripherals. The 8-bit external bus V20 and full 16-bit V30 fit into most existing systems and upgrade performance substantially.

The V20 and V30 feature dual data bus architecture and other hardware refinements to provide outstanding speed. The 101-instruction set includes bit operations, bit field operations, packed decimal operations and stack manipulations. Power consumption rates a low 300mW in operation and 50mW for standby.

Comprehensive CMOS peripherals complement CMOS V20/V30. A CMOS coprocessor (floating point processor) and advanced DMA controller are well under development.

System performance is further boosted with a multi-tasking Real Time OS. Development tools include an In-Circuit Emulator, Relocatable Assembler, Pascal and C compilers.

The V20 and V30 are to be alternately sourced by Zilog Inc., and Sony Corp.



LARGE-CAPACITY INFORMATION DISPLAY PAGER.

The new NEC D4α Information Display Pager packs state-of-the-art technology into a credit card-sized unit weighing only 100 g (3.5 oz).

It receives, displays, and saves a total of 12 messages up to a maximum total of 416 characters. The maximum single message length is 352 characters. Each message appears on the 5 x 7 dot matrix Liquid Crystal Display (LCD), 16 characters at a time. These features enable detailed messages or instructions to be communicated to the IDP user.

Up to eight current messages can be saved and recalled from



the PORTAL memory. An additional four important messages can be selectively shifted to the VAULT memory, which protects them from being overwritten.

The two unique addresses assigned to each unit provide both information display and priority tone-only services to the users.

One of four optional alert modes is selectively programmed into

each unit. The "Silent Secretary" mode delays received messages until it is convenient for the user to review them. Also, the number of messages

received while in

this mode will be displayed on the LCD. "Visual Alert", with a blinking red LED, displays and saves incoming messages in memory. "Quiet Alert" sounds a low-level alert tone. "Vibration Alert" blinks the LED and vibrates while it displays and saves incoming messages.

NEC TO SUPPLY FIVE EUTELSAT AND TWO SMS EARTH STATIONS.

As part of the European Communications Satellite (ECS) System, NEC is supplying earth stations for five member nations of the European Telecommunications Satellite Organization (EUTELSAT). Austria, Portugal, Switzerland and Turkey have ordered complete satellite communications systems, including TDMA/DSI (digital speech interpolation) terminal equipment. NEC has already supplied to Belgium a high-performance 18-meter diameter dish antenna and low-noise

amplifier subsystems.

The latest digital technology will be used for telephone transmission to effectively use satellite transponders. The TDMA/DSI system will permit each station to transmit for a fraction of a second using the whole bandwidth of the transponder. The EUTELSAT series of satellites also forms a special network called the Satellite Multi-Service (SMS) System primarily for business users. NEC has also received orders for two SMS and two TV uplink earth stations from Norway.

NEC
NEC Corporation

NETWORK SYSTEMS HANGS TOUGH WITH LAN RIVALS

Company that dominates market for computer-center networks goes to court to thwart competitors

Minneapolis

The granddaddy of networking companies does not intend to yield any ground to its younger competitors. Network Systems Corp. has risen above the networking crowd by concentrating on the industry's largest and most sophisticated computer users and by protecting its technology—to the point of suing its rivals.

The 11-year-old company shipped its first high-speed Hyperchannel network in 1977. Using the most advanced emitter-coupled-logic technology available, Hyperchannel ran at a blazing 50-Mb/s clip. It still does. Today, Hyperchannel has become a de facto standard to link high-speed network supercomputers, mainframes, lower-level processors, and peripherals—often geographically dispersed, and all from different manufacturers.

Networking is one of the hottest businesses in computers, with about 300 vendors trying to link everything from personal computers to mainframes to minicomputers. Many of Hyperchannel's younger peers in networks are chasing the market for linking dispersed personal computers and work stations.

But "we start at the computer center" where the need is for higher-performance host-to-host systems, says Lyle D. Altman, Network Systems' 55-year-old president and chief operating officer. Altman, like Network Systems' 59-year-old cofounder, chairman, and chief executive officer James E. Thornton, had worked at Control Data Corp. and other computer concerns. Thornton designed supercomputers; Altman, a certified public accountant, came from the marketing side.

Using the same basic design on which work was started in 1974, Network Systems has since brought out adapters so that Hyperchannel can connect processors from over 30 different companies. Link adapters further extend the line to allow communication among dispersed Hyperchannel networks with terrestrial or satellite communication lines.

"It's really quite amazing. They've



Litigious. Chief Lyle D. Altman says Network Systems Corp. sues when it has "a legitimate reason."

had a product with a life cycle of 10 years," observes Gary Smaby, vice president and senior technology analyst at Piper Jaffray & Hopwood Inc., a Minneapolis investment company. Virtually without competition, Network Systems has carved out what appears now to be a nearly impenetrable niche in the extreme high end of the mixed-vendor network market.

Because of this enviable position, the company has kept revenues and profits growing at better than a 50% annual clip for the past six years. And the current computer industry slump has so far shown no signs of slowing this trend.

Network Systems added 38 new accounts in the first quarter this year alone, and saw sales and profits grow by 52% and 61%, respectively, over last year's first quarter. That's on top of 51% and 56% growth last year, when 1984 sales and profits totaled \$71.2 mil-

lion and \$15.6 million. "Network Systems is one of the few companies I follow that's going to meet their aggressive forecasts for the [current] quarter," says Smaby. He projects company growth of over 50% this year and 40% to 45% over the next three to five years.

As the only game in town for high-end networks, Network Systems has also been able to keep Hyperchannel's margins high, which hasn't escaped its customers. "I think the price ought to be about half of what it is now, and they could still make a profit," says Gary D. Mays, a software engineer for teleprocessing at General Dynamics Corp.'s Central Data Services Center in Fort Worth, Texas.

Prices up. "Network Systems has definitely had a monopoly on this type of networking in the past. They are probably one of the few companies where prices have continued to go up instead of down," observes Wayne L. Hanna, program manager for computer-aided design and manufacturing for McDonnell Douglas Corp. in St. Louis. "I think they need a little competition."

Hanna may soon get his wish. Just down the street from Network Systems in the suburb of New Hope is a new company, Computer Network Technology Corp., looking to crack the lock held by its established competitor.

CNT's forthcoming Lanlord High Speed Networking System will take dead aim at Hyperchannel. Based on current generation microprocessor technology, the Lanlord network will equal or better the message throughput of the 10-year-old Hyperchannel, CNT claims [see related story, p. 49]. And at about \$25,000 per node, it will sell for about half the price of a Hyperchannel.

"Network Systems has built a marvelous company and done very well," says Robert A. Lutnicki, CNT's vice president of marketing. "But the fact is, they've left themselves very vulnerable to competition. They're a one-product company. Over 90% of their sales revenue last year came from one product, and that product is 10 years old."

Though Lanlord adapters can't plug directly into a Hyperchannel network, they will run with any software written for Hyperchannel, CNT says. The start-up hopes to pick off some business from current Hyperchannel users that are setting up new, separate networking installations. In addition, says Lutnicki, the improved price-performance ratio of the Lanlord may clear the high-speed networking path for users of minicomputers and other smaller machines who cannot justify the cost of a higher-priced Hyperchannel network.

CNT had better tread carefully, though. Network Systems derives about half of its Hyperchannel sales from its

existing base of over 500 customers. The company has moved aggressively to protect its position, filing lawsuits against potential competitors. Some observers say that abuses the legal system for marketing purposes.

The first example was a 1983 suit against Masstor Systems Corp., Santa Clara, Calif., charging trade-secret, patent, and copyright infringement. This drew a countersuit from Masstor charging misuse of the legal system. But the dispute was settled last year when Masstor agreed, among other conditions, to drop its plans to build Hyperchannel-compatible hardware and become an original-equipment manufacturer for Hyperchannel adapters.

Kenneth Thurber, president of Architecture Technology Corp., a LAN consulting and newsletter-publishing firm in Minneapolis, criticizes the Masstor suit and a second action filed by Network Systems last January. In that case, which is still pending, Network Systems is charging breach of contract against Megabit Communications Inc., Minneapolis, and its founder, a former Network Systems employee.

"Almost two years ago, we ran a bunch of articles in our newsletter about forthcoming competition for Network Systems," Thurber says. "And the way that Network Systems solved that problem is they went to the courts. I don't think it's feasible for a high-tech company to survive when it fights in the courts instead of in the streets. They should be fighting on the technology front instead of in the courts."

At Network Systems, Altman declines to discuss details of the two suits. But he bristles at questions about misusing the legal system. "There's a whole lot of

other people that we haven't filed suit against. We've only filed suit where there's a legitimate reason to have done so," Altman says. "If somebody stuck his hand in your pocket, would you leave it there until he stole everything or get it the hell out of there?"

Network Systems is working to protect its position on product-development and marketing fronts, too. It broadened its base in 1983 by introducing a 10-Mb/s network known as Hyperbus, which can also be linked to a Hyperchannel.

Though Network Systems was almost exclusively a hardware supplier that left software development up to its customers, the company has also moved aggressively in this area with its host-based Netex package. Netex works with some 30 different operating systems to drive a Hyperchannel network. The total is expected to reach 40 operating systems by the end of the year.

First test installations are also set this year on an advanced new fiber-optic network product called Datapipe that will run at an unprecedented 275 Mb/s. [*Electronics*, July 8, 1985, p. 12]. Datapipe is positioned as the backbone to tie together multiple Hyperchannel/Hyperbus networks into what Altman calls "global networks."

Even if the going gets more competitive, few observers doubt that Network Systems has the wherewithal to fight both a pricing and new technology battle. Explains Thurber, "Network Systems is the biggest LAN company today and that says something for them. It means they are tough and they are savvy. We can disagree with the way that they have done it, but by all standards they are the No. 1 company in networking."

—Wesley R. Iversen

BOTTOM LINES

BONUSES GET BIGGER FOR HIGH-TECH EXECS

Because of the employment turmoil in the high-tech industry, companies may not need to pay bonuses to attract technical workers. But they are using increased incentives to lure top managers. According to a survey on benefit comparisons among high-tech companies conducted by the Hay Group, human-resource management consultants in Philadelphia, more than 75% of respondents use some form of recruiting bonus at the upper-management level, compared with 8% of industrial companies overall. The most popular bonus is the one-time front-end reward, usually cash, stock options, or a combination of the two. The Hay Group notes that the same business instability that makes technical help easier to hire "will probably make it even more important—and difficult—to obtain the services of top managers. Look for executive hiring incentives to remain prevalent in high tech."

And look for high technology to continue its fast pace in hiring senior level execs. According to a new survey by Korn/Ferry International, executive recruiters based in New York, recruiting among high-tech companies rose to 19% of national executive demand in this year's second quarter, up from 17% a year ago. Companies are hiring top managers "to tackle the critical financial and market difficulties surfacing in today's economy," the firm said. Areas such as corporate planning and strategy, manufacturing cost effectiveness, and inventory and materials systems "are now assuming importance."

Building bridges. Hyperchannel adapters can link processors from 30 different vendors.



DU PONT UNIT INVESTS \$32 MILLION IN BRAZIL

The Brazilian subsidiary of E.I. du Pont de Nemours & Co. plans to invest \$32 million over the next five years to make connectors and integrated-circuit layout film. A Du Pont spokesman said the company's objective is to double (from the current 14% share) its participation in Brazil's connector market.

JUPITER TECHNOLOGY RECEIVES FINANCING

Jupiter Technology Inc., a Waltham, Mass., company that is developing a system to let information-processing equipment from different vendors communicate and share information, has received \$2.25 million in its first round of venture financing. The company said the funds will be used to continue engineering activities and to expand marketing efforts.

COMPACT-DISK SURGE BOOSTS WINEY'S MAGGIES

White Bear Lake, Minn.

James M. Winey, a longtime audiophile and inventor who turned his hobby into a thriving business, is happy about the current sales surge of compact disk players. CD use is sparking a turnaround in the audio industry.

And that means good news for Magnepan Inc. Winey's 16-year-old maker of high-end loudspeakers rebounded in sales last year after a two-year dive.

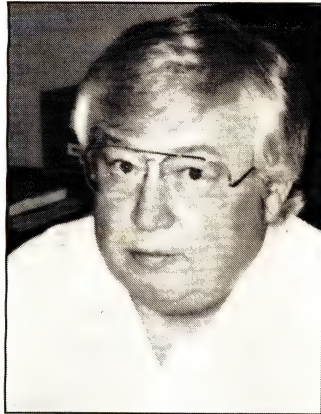
But Winey also says some surprising things about the new audio format. CDs are touted as superior to conventional analog long-playing records in terms of sound reproduction and durability. Yet Winey claims a CD player still can't match the performance of a no-holds-barred analog system. "If you get everything optimized, an analog record still sounds better, if it's a good record," Winey contends.

Aural quest. The 51-year-old Iowa-born entrepreneur should know. He's been stalking the ultimate sound since he caught the audio bug in the late 1950s as an undergraduate industrial engineering student at Iowa State University. That longing ultimately caused him to quit his job as a field engineer at 3M Co. in 1969 to found Magnepan.

Working with \$50,000 invested by friends and relatives, he spent two years in a shop behind his house in this St. Paul suburb perfecting the speaker design that he ultimately marketed and still tinkers with regularly. Today, Magnepan has about 50 employees.

Winey's speakers are as unconventional as his views on CD technology. Known affectionately as "Maggies" by some in the trade, Magneplanar speakers look more like room dividers than stereo gear. Only 2 in. thick and built in panels that are 18 in. wide and up to 6 ft. tall, the speakers work on a unique, planar-magnetic driver principle for which Winey holds five patents.

Unlike standard box speakers, which rely on a cone that moves under impulse from a voice coil, Magneplanar speakers use a stretched sheet of Mylar as a diaphragm, to which a zigzag grid of aluminum wire or foil is attached. The grid is close to another plane that carries a series of elongated calendered or extruded magnets. When signal current



Audiophile. Magnepan's Winey likes the new audio revolution.

from an amplifier is fed through the grid, the resulting magnetic-field interference causes the diaphragm to vibrate, producing sound in accordance with the signal.

The result, says Winey, is a speaker that projects sound in all directions and from the entire plane of the vibrating diaphragm. Magneplanars thus produce superior musical "height" and realism, he contends, and are

immune to the distortion from sound-wave containment or transient-induced cone flexing that plagues conventional speakers. Magneplanars cost between \$500 and \$3,700 per pair.

Winey concedes that CD technology will eventually outperform even the most finely tuned analog systems. But Winey is much more excited about a long-term sales boost from the push toward sophisticated, integrated audio-video systems. "In audio-video, the emphasis has got to be on the audio, and it doesn't take much imagination to see our speakers being used as the doors on a video cabinet." —Wesley R. Iversen

SCHWARTZ PUSHES COLUMBIA'S ROLE

New York

Since April, when the National Science Foundation chose Columbia University as one of six U.S. engineering research centers, the telecommunications industry has been taking note of its research potential. There are over 1,700 telecommunications companies within a 50-mile radius of the former home of the Manhattan Project.

Helping the university gain notice is Mischa Schwartz, a professor of



Educator. In his role as director of Columbia's CTR, Schwartz stresses education as well as research.

electrical engineering and director of Columbia's new Center for Telecommunications Research (CTR). Schwartz maintains the NSF designated his university because of its early work in computer communications. The Columbia center will receive \$20 million from the NSF over the next five years [*ElectronicsWeek*, April 22, 1985, p. 31].

In addition, Schwartz says the School of Engineering and Applied Science received a \$500,000 Department of Defense grant three years ago to improve laboratory instrumentation. That money, along with support from New York state, was parlayed into the CTR. Now Schwartz hopes the NSF funding will attract industry funds.

Though prospective industrial affiliates have inundated him with phone calls, Schwartz, 58, still manages to teach one course and oversee the work of seven doctoral students. That dual dedication to research and instructing applies to his running of the center.

Schwartz admits the center's primary objective is to conduct basic research in telecommunications, but he is quick to add that it is also designed to produce engineering graduates trained in telecommunications technology. Evidence of Schwartz's commitment to that goal hangs on his office wall—an education award from the Institute of Electrical and Electronics Engineers that he received in 1983.

Open house. Despite the center's mandate from NSF to enhance the international competitiveness of U.S. industries, Schwartz doesn't want to exclude international participation in the CTR. Though he acknowledges the concerns of prospective U.S. industry affiliates, the professor maintains that part of its role is to "provide neutral territory" for competing companies and to promote an atmosphere for the free exchange of scientific information.

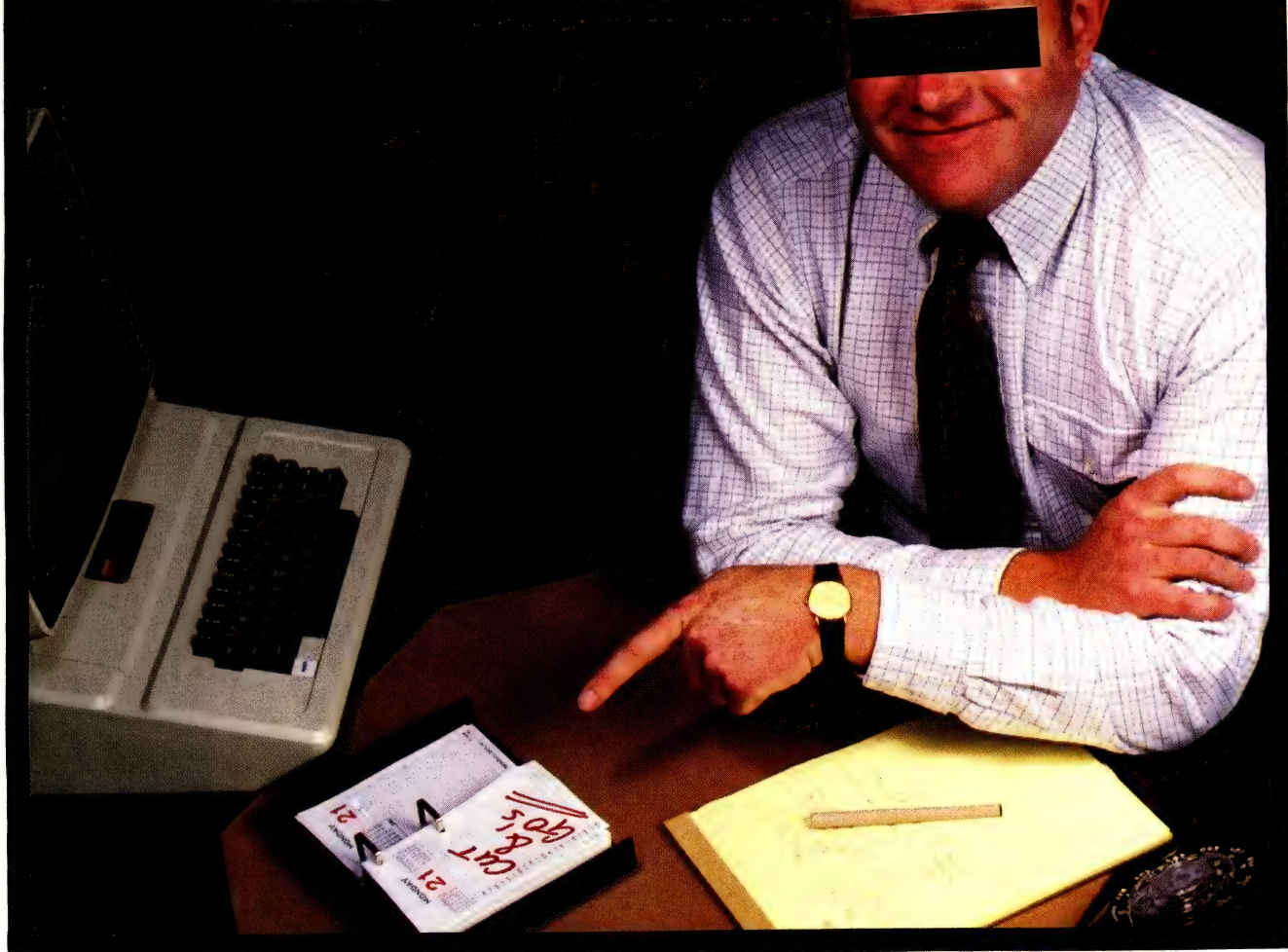
Schwartz sees the CTR's chief challenge as this: "How do we build networks of the future that are as ubiquitous as the telephone is today?" To find the answer, the center is organized into four major areas of research: systems

and new concepts; very large-scale integration circuits and architectures for telecommunications; microelectronics and electro-optical devices; and analytical studies.

In addition, faculty and graduate researchers will use a flexible network testbed—Magnet—that can support data, graphics, and voice and video communications. —George Leopold

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A CHIP BUSINESS THAT IS STILL GROWING

by Bernard Conrad Cole

INNOVATION SPURS MARKET

FOR APPLICATION-SPECIFIC INTEGRATED CIRCUITS

Though the semiconductor industry today resembles a barren wasteland where little grows and only the fittest survive, one fertile oasis remains. Makers of application-specific integrated circuits have been relatively untouched by the economic woes—lower earnings, mounting inventories, chronic quarterly losses, layoffs, and shutdowns—that have beset the major makers of standard ICs.

There is nothing like a free-spending market to spur innovation. Thus change is occurring at an almost logarithmic rate in the ASIC industry, an international conglomeration of large and small gate-array and standard-cell vendors, full-custom houses, foundries, and software developers. Competition is especially frenzied among manufacturers of standard cells and gate arrays in all areas from process and circuit technology to design methodology.

The semiconductor industry as a whole has a book-to-bill ratio of 0.6:1, but the ASIC portion—custom, semicustom, standard cells, gate arrays, and programmable logic arrays—is doing much better at about 1:1, according to Andrew Prophet, industry analyst at Dataquest Inc., San Jose, Calif.

At present, ASICs constitute about 12% to 15% of the total IC market. For 1985, Prophet estimates that market will be \$1 billion in sales for gate arrays, about \$140 million for standard cells, about \$200 million to \$250 million for programmable logic circuits, and about \$1 billion for full-custom ICs. By 1990, the ASIC share of the total IC market should double to about 25% to 30%.

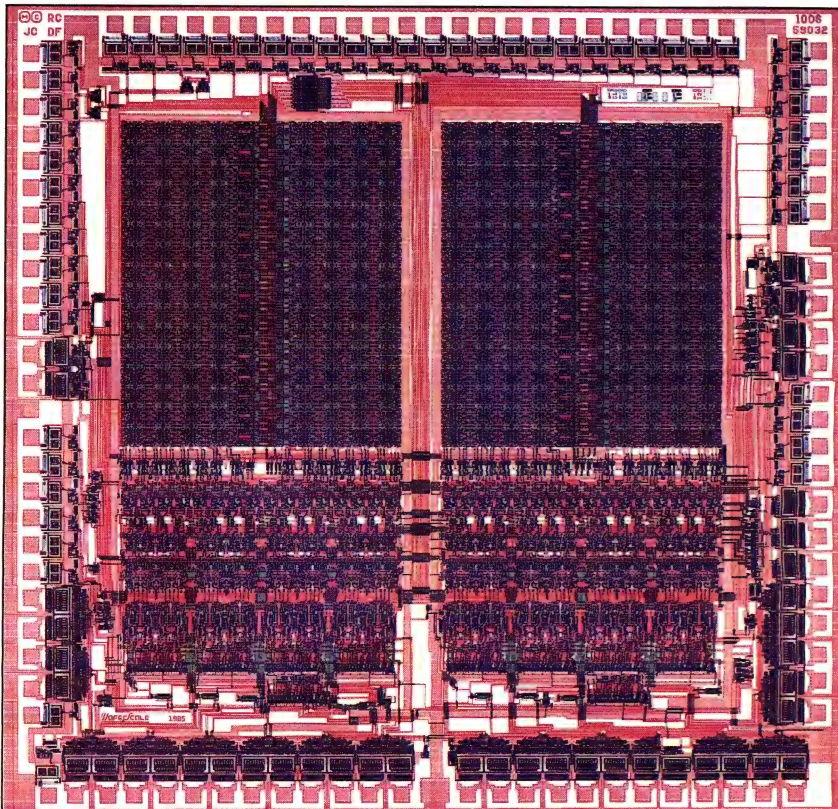
Gate arrays will still command a large portion of the ASIC market, he says, growing to almost \$3 billion in sales. But they will no longer dominate the semicustom side of the ASIC business, as standard cells will grow almost twentyfold, to about \$2.5 billion. PLAs will also grow dramatically, increasing almost fourfold, to about \$900 million, by the end of the decade.

But full-custom circuits will not disappear, says Prophet, predicting growth of almost 80%, to \$1.8 billion. His projections are borne out by similar numbers from Integrated Circuit Engineering Corp., Scottsdale, Ariz., which estimates that the total ASIC market will grow from \$1.6 billion in 1984 to almost \$8 billion in 1990. Its projec-

tions show that though full custom will do more than hold its own, almost quadrupling from \$775 million to \$2.5 billion, the most dramatic growth will occur in the semicustom portion. ICE projects that gate-array sales will grow from \$455 million to \$1.4 billion and sales of programmable logic from \$250 million to \$1 billion. The market for standard cells will make the steepest increase, from a mere \$90 million in 1984 to \$2.5 billion in 1990.

As in memories, n-MOS is virtually extinct in the ASIC market as a process technology. Most current and future designs are in either CMOS or some form of advanced bipolar implementation. Manufacturers of ASIC semicustom gate arrays and standard cells have made impressive progress in increasing gate complexity and circuit density.

In CMOS, the vast majority of designs in production are implemented using 3- to 5- μ m design rules. But there is an increasing shift to 2 μ m by gate-array companies such as LSI Logic Corp. and California Devices Inc. and by standard-cell vendors such as Texas Instruments, General Electric, and Zymos. In gate arrays, this has allowed circuit densities of 10,000 to 20,000 gates—25,000 gates in standard-cell implementations. Gate delays approaching 1 ns are typical and 500 ps



1. Big cell. Representative of the growing complexity of standard cells is Waferscale Integration's 59C032 32-bit microprocessor cell. It contains eight elements functionally identical to a 2901 microprocessor based on 4-bit slices.

are maximum; these allow flip-flop frequencies in the 60-MHz range and fully loaded system-clock speeds of 30 to 35 MHz.

Though this kind of performance encroaches on the lower end of that for bipolar gate arrays, vendors such as Honeywell, Fairchild Semiconductor, Applied Micro Circuits, and Motorola have speeded up their offerings by shifting to higher-speed bipolar processes such as emitter-coupled logic and current-mode logic. Besides allowing typical gate delays of 200 to 300 ps, densities approaching 10,000 gates are now possible.

Gallium arsenide ASICs are also now emerging from vendors such as Tektronix, Harris Semiconductor, and Vitesse Electronics. Though their gate densities are still rather modest—from 1,000 to 2,000 gates—their speeds are greater—under 200 ps. Moreover, this improvement in speed comes at the same power as equivalently sized CMOS circuits and matches the speed of ECL, CML, or TTL gate arrays at much lower power levels.

The name of the game in the ASIC market, as in all the semiconductor industry, is improved speed and density but at the lowest possible cost per transistor or function. Thus even though shrinking geometries increase density and speed, ASIC makers are loath to reduce geometries much below 2 μm at present because doing so would require increased capital costs for new fabrication equipment.

One way to get around this problem is to increase the number of metal layers used for device interconnection, permitting more efficient layout. Though manufacturers of bipolar gate arrays have used two and three levels of metal for many years, dual-metal interconnections are only now becoming common in CMOS. However, a few companies are experimenting with three levels of metal to make better use of the arrays and facilitate automatic circuit placement and routing.

In a 24,000-gate array from Toshiba Corp., Kawasaki, Japan, for example, the first layer supplies the interconnections within the cell and to power supply and ground. The second and third levels are used for intercell wiring. By covering the first level and the substrate with an insulator, the upper two levels can be run over the cells, eliminating the need for

dedicated wiring channels for global interconnections.

Alternatively, a number of companies, such as Waferscale Integration Inc., Fremont, Calif., are experimenting with the use of metal and metal silicide combinations to eliminate the need for the extra chip area in the circuit usually dedicated to metal-to-metal connection holes through the oxide insulation layer (Fig. 1).

Full custom has held its own against semicustom until now because it fully utilizes all the chip's silicon resources, with no wasted transistors and no unnecessary interconnections. To overcome this advantage and allow them to fabricate increasingly complex devices, semicustom ASIC manufacturers have turned to a variety of methods to reduce or even eliminate wiring channels.

A straightforward way to do this is Waferscale Integration's Probe standard-cell library, which uses variable-height rather than fixed-height cells. Standard fixed-height cells waste considerable silicon because the wiring tracks are not of uniform size; in the variable-height approach, the cells can extend into routing areas not filled with interconnections.

Some design approaches, applicable to both standard cells and gate arrays, include extra transistors in the wiring channels and others eliminate the channels totally.

Sea of gates

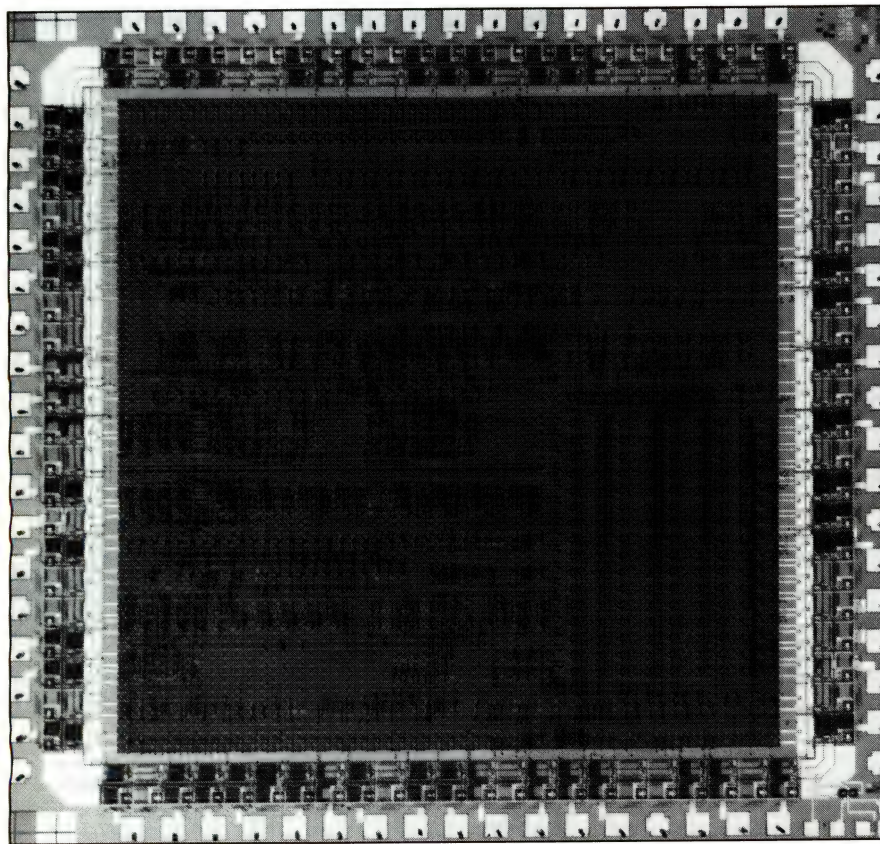
One of the most interesting of such approaches is the sea-of-gates array developed by LSI Logic, Milpitas, Calif. Chips fabricated with its 2- μm H-CMOS double-metal process (Fig. 2) contain a central area consisting of densely packed cell columns with no predefined first-metal routing channels. After logic design and simulation, macrocells are placed by computer-aided-design layout and input/output pads are assigned.

The number of tracks required for optimal routing is computed and allocated by the CAD layout system, rather than by predefined design. First-metal routing is achieved by running metal over the cell columns rather than in predefined channels on a field oxide, which is more conventional.

The chief advantage of this approach is that the number of tracks in each channel can be adjusted, making it easier to achieve 100% autorouting and near-100% gate utilization. Indeed, close to a threefold improvement in internal gate density is possible.

Another approach, developed by California Devices, San Jose, uses what it calls channel-less architecture (Fig. 3), which can be adapted to either gate-array or standard-cell designs. A major advantage of this approach is that areas with routing congestion can be assigned additional wiring resources by selectively placing empty unit cells to provide maximum routability per unit area, says Jamie R. Martin, strategic marketing manager at the company.

In this approach, the wiring resources for global interconnections are folded over onto the active gate or cell area. Used in gate arrays, such channel-less architecture accommodates almost 100% more gates per unit area than conventionally routed arrays. For example, Martin says, 3- μm channel-less arrays consume 30% less circuit area per gate



2. Sea of gates. LSI Logic fabricated an experimental 2- μm H-CMOS array in which first-metal routing is achieved by running metal over the cell columns. Typically, metal is run in predefined channels on a field oxide.

than 2- μ m gate arrays with dedicated interconnection areas. In a standard-cell implementation, this approach yields chips 20% to 40% smaller than ones built with traditional structures.

Taking a slightly different tack is Fujitsu Ltd., whose channel-less array contains about 30,000 cells. Each of these cells can be implemented as either a logic or memory element. In this design, the basic cell has four normal and four smaller transistors.

The normal transistors have separate source and drain regions; the smaller transistors have common source and drain regions. All eight structures are used to fabricate an eight-transistor static-random-access-memory cell; logic circuits would use only the four normal-sized transistors. The space over the four unused smaller transistors is then used for wiring channels. Similar channel-less designs are now also emerging from companies such as TI, Mostek, and Hughes Aircraft.

From standard cells to supercells

With chip densities equivalent to 50,000 to 100,000 transistors (10,000 to 25,000 gates) now possible, semicustom-ASIC companies face both an opportunity and a problem. At these densities, it is now possible to truly design a complete system on a chip, with the resultant improvements in speed and reductions in component count and cost, says Dave Guzeman, marketing vice president at Zymos Corp., Sunnyvale, Calif. But the problem is that even with the most advanced CAD tools, designing at the gate or even the macrocell level is not enough to maintain the faster turnaround time associated with full-custom designs.

Standard-cell vendors have been the first to rise to the challenge with the introduction of larger subsystem-level building blocks—variously called megacells, supercells, or metacells. Initially, this has involved providing various compiled small- and medium-scale-integration logic and memory functions (including PLAs, static RAMs, and read-only memories) as higher-level building blocks. Within the last year or so, an increasing number of vendors have begun offering various

large-scale-integration functions—core processors, peripherals, and various specialized telecommunications and I/O functions.

Such megacells or supercells expand the limits of ASIC to the VLSI level by providing a mechanism for rapidly implementing complex functions within a single chip design [*Electronics*, July 15, 1985, p. 56], says Alex Young, Zymos's engineering vice president. Using megacells, the designer is no longer limited to off-chip components or a lengthy design process to include such functions as disk controllers, counter timers, microprocessors, and universal asynchronous receiver/transmitters, says Douglas Fairbairn, vice president of design technology at VLSI Technology Inc., San Jose.

An early approach to creating megacells that is still in common use is to make their physical structures closely resemble those of the standard chips from which they are developed. Such megacells generally retain the rectangular shape of the die intended for bonding into a dual in-line package. Similarly, I/O connections are situated for efficient package bonding and assembly.

Though this approach to megacell implementation has been a convenient way for vendors to develop new elements for their libraries, it does not make the most efficient use of silicon. Moreover, as ASIC designs approach VLSI levels, many vendors find that this approach can complicate layout and interconnection.

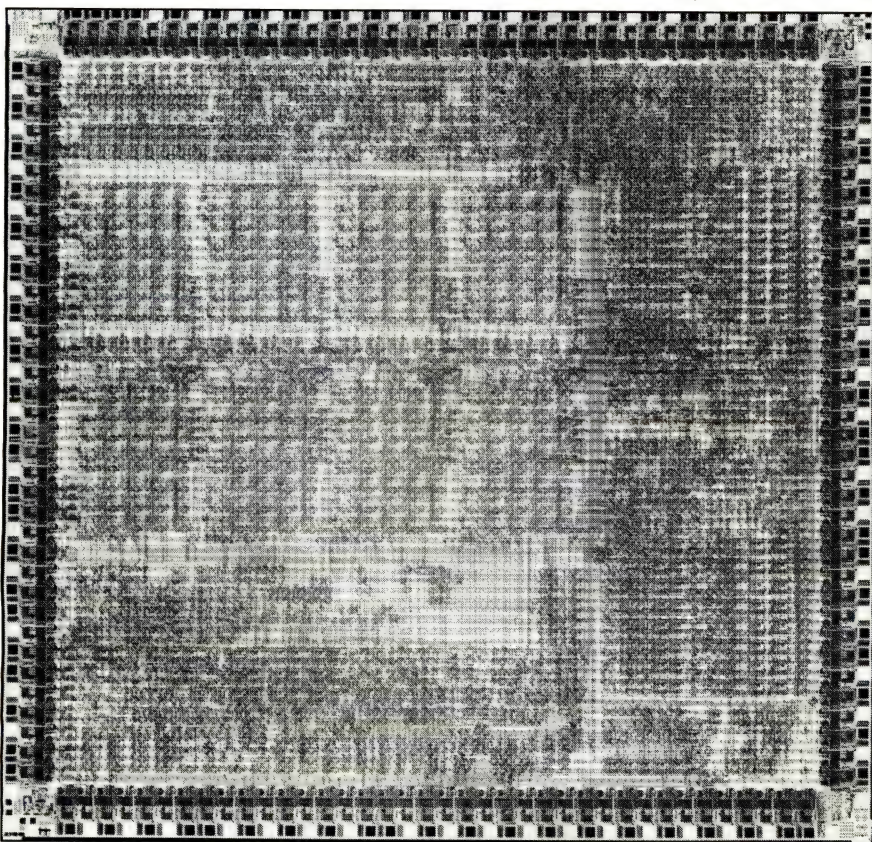
As a result, many companies are rethinking their approach and, like VTI, are designing functions for megacells. In VTI's approach, the megacells have a standard height and vary only in width. This allows them to be organized in an orderly manner that conserves chip real estate and simplifies chip layout, according to Fairbairn.

To further optimize chip area and reduce design time, VTI interconnects its megacells with other megacells and on-chip compiled RAM, ROM and PLAs by means of a special address and data-bus architecture. Called Megabus, this architecture has predefined signals and timing as well as a physical organization common to all megacells. With this approach, the designer can efficiently combine multiple megacells on a single chip using additional cells compiled from its libraries and rapidly develop complex VLSI circuits.

One measure of the increasing power and sophistication of the supercell/megacell approach is the evolution of the various core processors available. Virtually every standard-cell vendor now has available a 4-bit core-processor megacell built around one of several popular standard microcontroller families such as National Semiconductor's COPS family.

At the 8-bit level, the 6502 architecture has become common, as has the 80C48 and 80C51. Bit-slice processors based loosely on Advanced Micro Devices Inc.'s 2900 family are also being incorporated into standard-cell libraries, offering CMOS performance approaching that of low-power Schottky TTL bipolar technology. Also becoming popular are core-processor megacells based on more sophisticated 8-bit central-processing-unit designs, such as the Z80-based standard cells now being offered

3. No channels. In California Devices' channel-less architecture, instead of providing dedicated interconnection areas, global interconnections are folded over onto active gate or cell areas. This is a 10,000-gate array.



by VTI and Gould AMI, Santa Clara, Calif., and the 8085 being planned by Oki Semiconductor, Sunnyvale, Calif. Oki also plans to introduce a 16-bit processor megacell based on the 8086. In addition, National plans to produce core processors built around many of its standard 8-, 16- and 32-bit CPUs.

A few standard-cell companies are taking the megacell concept even further using these high-level functional blocks to create even larger building blocks—metacells, as it were. The best illustration of this trend comes again from the core-processor area, with the introduction by Waferscale Integration of its 59C032 cell, a 15-MHz, 32-bit core processor built from four bit-slice building blocks in its existing library.

Containing eight processing elements functionally identical to bipolar 2901C bit slices and three 2902 equivalent carry/look-ahead units, the cell replaces at least 11 discrete bipolar ICs when used in a semicustom chip. This 32-bit cell measures only 0.15 by 0.15 mils, which the company says is roughly half the size of most stand-alone 32-bit processors. The cell's small size permits incorporation of other cell-based functions such as RAM, ROM, erasable programmable ROM, PLAs, or random logic onto the same chip.

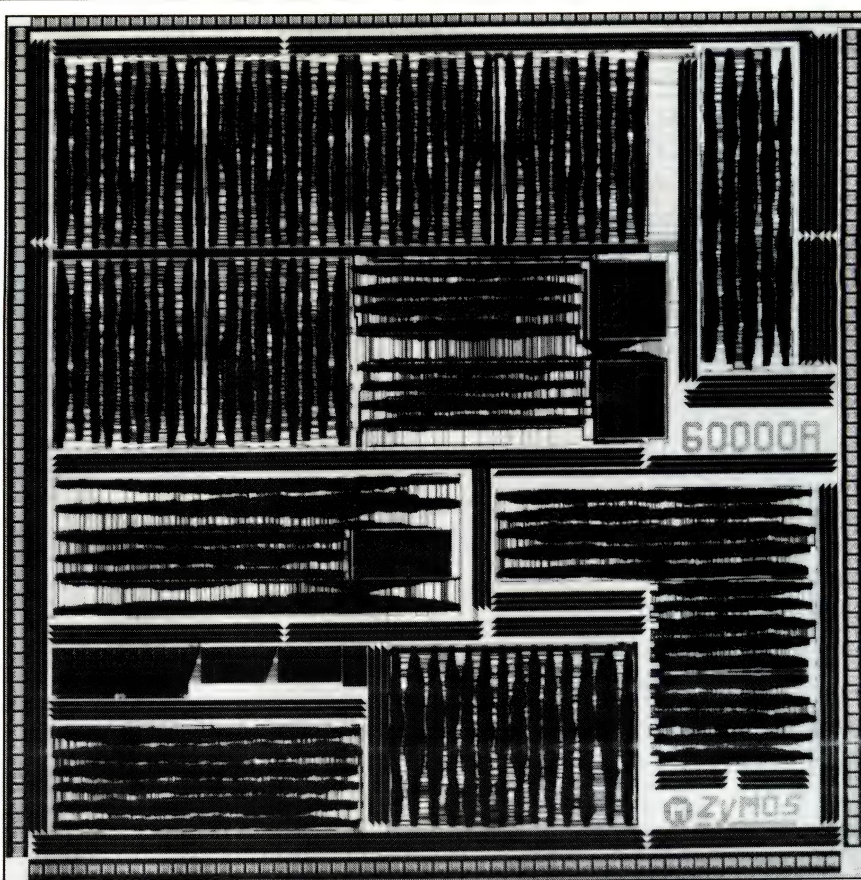
Yet another indicator of the growing sophistication of the megacell is the emergence at many companies of what can only be called the silicon-spreadsheet approach to chip design. The approach is analogous to the spreadsheet used in financial modeling, which allows users to do what-if projections of numbers and data before actually printing out the results. Typical of this approach is that used in the UK by The Plessey Co. plc's Clark Research Center in collaboration with International Computers Ltd. plc's West Gorton design group.

Paracell approach

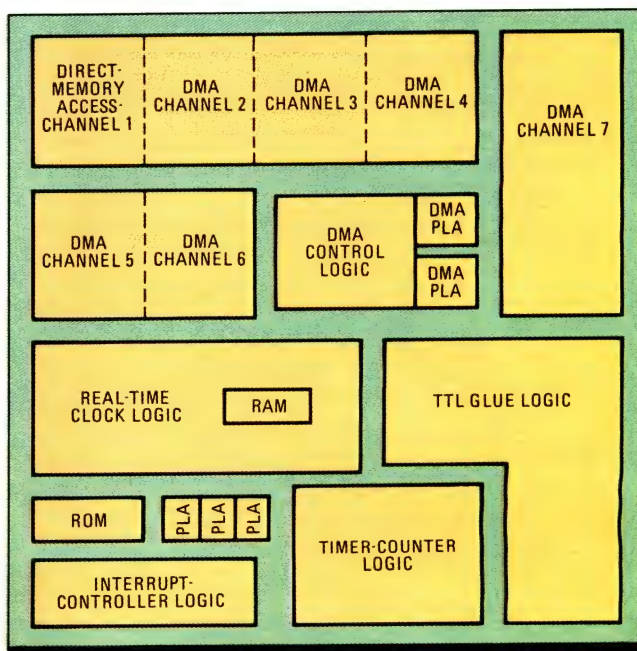
The two firms use combinations of RAM, ROM, PLAs, arithmetic-logic units, adders, comparators, content-addressable memories, register files, and autorouted gate arrays—called paracells—to automatically create designs customized to a designer's specifications. Parameterization software generates a set of primitive cells for each programmable function and stores them in a library with the assembly rules for constructing the overall function. This assembly software then automatically generates any new cells and adds them to the user library. A user can order any size of RAM up to 16-K or ROM up to 64-K, set the word width, and make the cells either square or rectangular to fit the available space.

System designers can specify the number of cells in the gate array as well as the number of cells in a row and the number of wiring channels between rows. They can also call up and specify the word lengths of PLAs, ALUs, and a variety of other paracell functions. Using these paracells, a designer can quickly assemble a wide variety of complex single-chip functions such as a 32-bit microprocessor, 16-by-16 multipliers, fast Fourier transform, butterfly functions, and floating-point coprocessors.

Zymos is taking the megacell concept one step further. The company has evolved the concept of the silicon template—a system-on-a-chip design, based on standard cells, residing in software that has been completely designed, simulated, and routed. Using silicon templates as frameworks, designers can

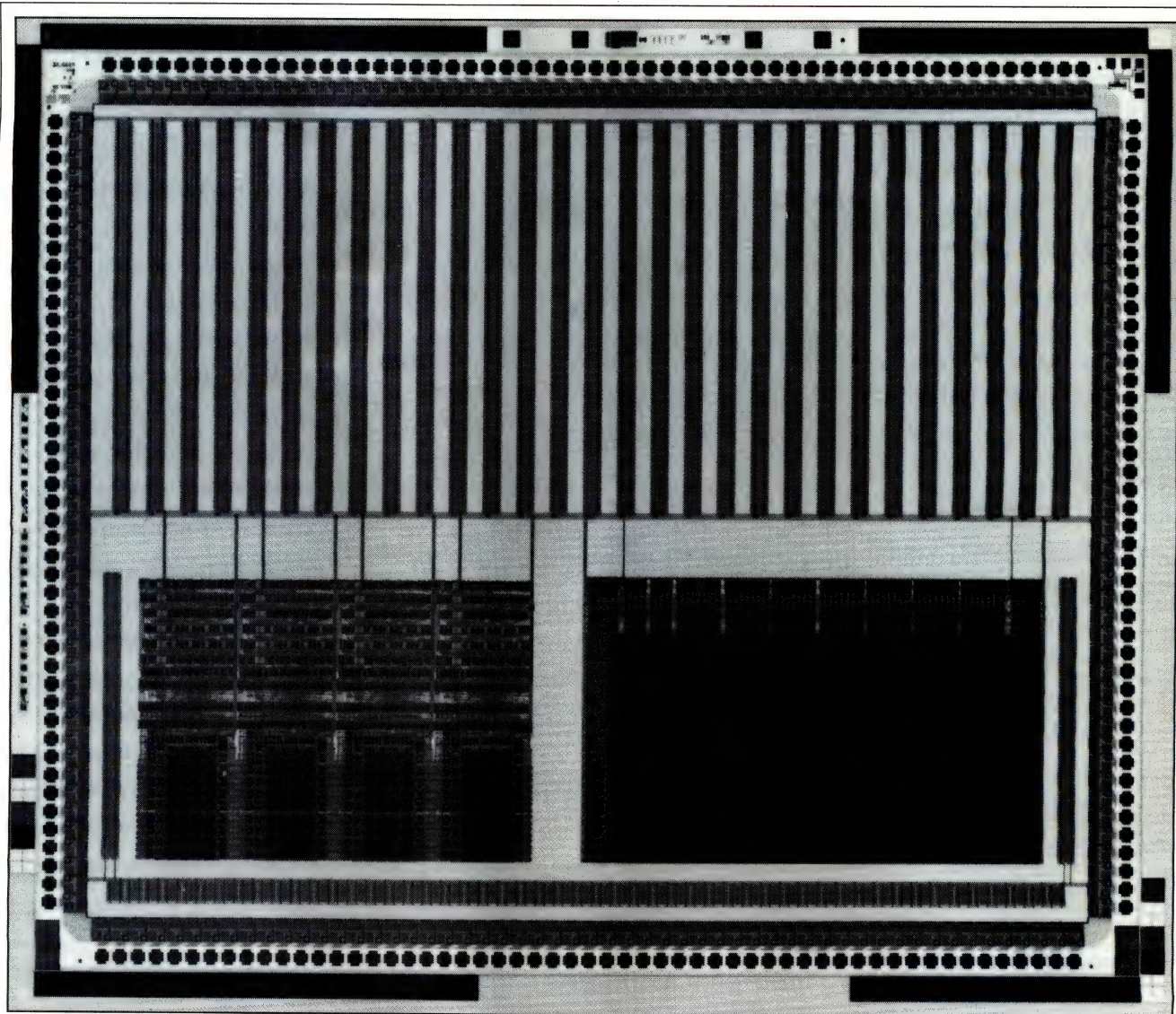


4. PC on a chip. In a silicon template created at Zymos, 87 of the 90 ICs making up the IBM Personal Computer AT motherboard reside on a single CMOS chip. A functional map of the chip appears below. The chip holds the equivalent of 25,000 gates.



enhance the performance of a particular system and/or customize it to their requirements in ways not possible with any other design approach.

A silicon template works in much the same way that a template for financial spreadsheet programs allows users to perform what-if projections. Using a silicon template allows similar manipulations of cells, megacells, routing alternatives, and feature additions and deletions within the context of a



5. Structured array. LSI Logic's LSA 2005 is a 2- μ m, 2-layer, metal-structured array comprising a 16-bit microprocessor slice, 32-K of configurable ROM, and a 4,000-gate logic array. Such chips can serve as powerful logic templates for certain applications.

system design before actually committing it to silicon.

Using its new 2- μ m 25,000-gate CMOS ZY-DP3 cell library and an enhanced Zyp Design Automation System, Zymos has developed such a silicon template for the IBM Corp. Personal Computer AT (*Electronics*, July 1, 1985, p. 23) that replaces 87 of the 90 LSI, MSI, and SSI logic circuits on the AT's 14-by-5-in. motherboard (Fig. 4). Except for the 80286 microprocessor, the 80287 coprocessor, the 8042 keyboard controller, the ROM basic I/O system, and the dynamic RAM, all the components have been reduced to a single 450-by-450-mil design containing 11,642 cells, 512 bits of compiled RAM, 4-K bits of compiled ROM, and 84 compiled PLA terms.

The total chip count has been reduced from 90 to four ICs, excluding ROM and RAM, according to Zymos's Young. Using the PC AT as a silicon template, the designer works within the framework of the basic motherboard design to improve performance, functionality, and cost.

For example, at the board level, the 80286 operates with separate, nonmultiplexed data and address buses. But many of the peripherals used on the board were designed to operate in the multiplexed environment typical of earlier CPU designs, Young points out. On the board, this requires the addition of many external TTL MSI devices to translate signals back and forth between the two modes.

"In the silicon template, the board design was implemented

directly without any modification," Young says. "One of the things a system designer could do is reconfigure the various peripherals to operate in a nonmultiplexed environment, using cell and supercell elements from the Zymos library, eliminating the need for additional TTL circuitry. This would further reduce chip size as well as improve overall PC AT system throughput."

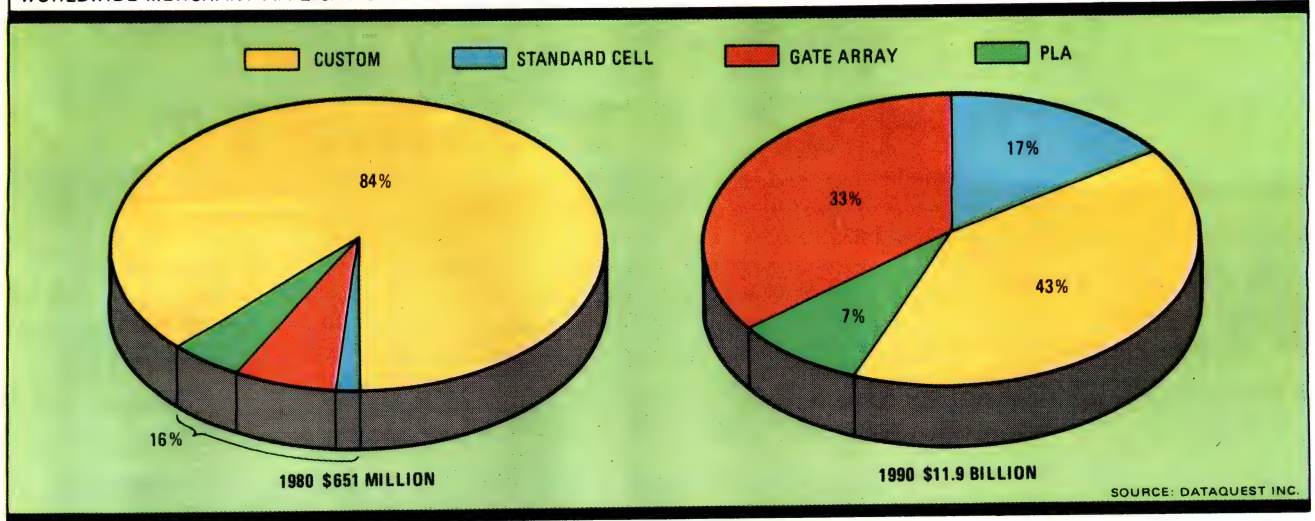
Similarly, by manipulating such other system parameters as peripheral word size, the number of timers, and the width and length of the timing elements, the designer can improve the system even further.

Structured arrays and logic templates

With the emergence of such approaches as the sea-of-gates concept and various channel-less architecture alternatives, the move to implementing gate arrays in larger and larger functional blocks is now under way.

Leading the way in this area is LSI Logic with its structured-array approach (Fig. 5). Using this concept as the starting point, the company is introducing a family of logic templates that combine its standard gate arrays with metal-configurable modules consisting of various combinations of RAM, ROM, PLAs, ALUs, and 2,901 megacells based on 4-bit slices.

The memories can be reorganized by means of metal-mask options; the blocks can similarly be interconnected to fit appli-



cations exactly. LSI Logic has identified about 20 such combinations of blocks and gate fields that it will offer as logic templates for specific applications, says Rick Rasmussen, structured circuits product manager at the company.

Among the first offerings are six logic templates in the LSA2000 series. Fabricated with the company's 2- μ m double-layer-metal H-CMOS process, they contain 3,000 to 6,000 uncommitted gates, 2,300 to 9,200 bits of RAM, and up to 32,000 bits of ROM.

The LSA2001, a general-purpose logic template aimed at a variety of electronic data-processing, telecommunications, and signal-processing applications, contains 3,000 uncommitted gates, a synchronous 16-bit ALU with ripple and full carry/lookahead functions, and 2-K of mask-configurable RAM that can be reorganized into word lengths of 4, 9, 19, and 36 bits as well as split into two separate RAMs. The LSA2002/2003 and 2004, Rasmussen says, contain various combinations of RAM and gate arrays, and are designed to allow system designers to tailor custom designs with up to 8 bits of RAM in various word widths.

The LSA2005 is the most architecturally interesting of the new logic templates, Rasmussen states. It contains a 16-bit microprocessor slice built from four 2901 megacells, 32-K of reconfigurable microcode ROM, and a 4,000-gate array. The LSA2007 is the last logic template and is aimed at general-purpose signal processing. It contains a 16-by-16 multiplier, 4-K of SRAM configurable in 4-, 9-, 18-, and 36-word lengths, and a 5,000-gate array.

The approach using structured arrays logic templates, says Rasmussen, offers several advantages over full-custom or standard-cell chips. "Rather than diffusing every layer of a chip, designers only customize two layers, which permits a faster turnaround for the production of prototypes."

Drawing on limited resources

If ASIC companies are optimistic now and enthusiastic about the long term, the prospects six months to a year or so away are making many in the industry nervous—and makes the oasis analogy all the more apt.

"Everyone is hoping for rain, assuming things will follow normal historical patterns," says Bruce R. Bourbon, vice president for semicustom products at Gould AMI. "But nothing about the current economic situation has been normal. So we can't afford to be certain about anything."

"If the slowdown in the economy continues much into 1986, beyond the first quarter, things could get bloody, outright ugly, in the ASIC market," says Dataquest's Prophet. "Even now, with things going pretty much their way, it is getting a little goosey for some of the thinly capitalized ASIC houses."

Bourbon lists a number of market factors that further complicate the situation. For one thing, the ASIC business is becoming much more international. Japanese companies, which are a growing factor in the gate-array business, are also moving into standard cells. Traditional gate-array vendors such as NEC, Toshiba, Fujitsu, and Oki Semiconductor are all considering moves in this direction.

In Europe, companies such as the Netherlands' NV Philips, Italy's SGS-Ates SpA, West Germany's Siemens AG, the UK's Ferranti, and Belgium's Mitec, in addition to the Société de Microelectronique in France, are moving into the semicustom ASIC sector—gate arrays and standard cells as well as bipolar and CMOS technology.

There is also a push, albeit a cautious one because of the depressed market, by industrial distributors such as Hamilton/Avnet, Schweber, Arrow, and Western Microtechnology into the ASIC business, providing front-end design support for certain ASIC offerings.

Though the total sales of ASICs will not be affected, the noncaptive ASIC portion is beginning to decline as original-equipment manufacturers do more of their design work in house. According to Bourbon, the large OEM customers want to regain total design control over their products and to lower nonrecoverable engineering costs. Thus as the design process gets easier, he says, OEMs will bring more and more design functions under their own roofs.

Even with an improving economy it is probable that there will be a shakeout over the next year or so, says Prophet. "There are simply too many companies in the ASIC business—at last count, 100 or so. That is just too many, no matter how big the market."

The winnowing out has already begun, he says. Several companies are believed to be on the verge of filing for protection from creditors under Chapter 11; others have been acquired (CAE Systems Inc. by Tektronix Inc. and Avera Corp. by NCA Corp.). Regional design houses have entered into strategic alliances with large silicon foundries such as Gould AMI and LSI Logic, and smaller software houses have merged with smaller hardware suppliers and foundries.

To protect themselves, many ASIC companies are entering into a variety of cross-licensing arrangements. Strategic alliances include those between Plessey and GTE Corp., Gould AMI and Mostek Corp., VTI and Zilog Corp., VTI and Fairchild, LSI Logic and AMD, LSI Logic and RCA Corp., National Semiconductor and International Microelectronic Products, TI and Fairchild, and TI and Signetics Corp. Such jockeying will continue until the economy sorts itself out, says Prophet. Needed are some indications of which way it will go: toward recession or toward growth. □

WILL TRON HELP JAPAN CATCH UP IN SOFTWARE?

Real-time operating system will give microcomputers supermini power

Momentum is building for TRON, a product that if successful could put to rest charges that software is a weak link in Japan's technological chain. The acronym, which stands for The Real-time Operating-system Nucleus, highlights the software's status as a base from which designers can build specialized, applications-oriented systems.

Since last November, Mitsubishi, Matsushita, Xerox Japan, and Canon have joined NEC as licensees. Prototypes supporting Motorola MC68000 and Intel iAPX86 microprocessors are ready, put together by TRON's developer, Ken Sakamura, a computer-science professor at the University of Tokyo [*Electronics-Week*, Oct. 8, 1984, p. 49]. One licensee envisions a low-cost commercial machine within a year. NEC Corp. is readying an array of TRON software for its machines. Both the university group and industry plan to continue to jointly support the project and expect to have full-blown, enhanced systems based on very large-scale-integration chips within three years.

The idea was to service a broad range of real-time functions in anticipation of future needs. In the future, Sakamura says, the most widely used computers will be small, high-performance personal units. He calls them "superpersonals"—personal computers with capabilities not far below those of today's supermini-computers. Sakamura believes that future machines will be used less for spreadsheets and word processing and increasingly for more stringent jobs.

At the same time, makers of these superpersonals will have to emphasize the cost advantage the machines have over larger units. This will make them attractive to users who need distributed processors and smart real-time data-gathering terminals. Today's garden-variety personal computer must evolve into a more serious machine, Sakamura says, one that can develop engineering-type applications in many areas.

To this end, he sought to construct an operating-system nucleus from which three unique types of full-blown operating systems—one each for industrial, business, and environmental control—could be built. The versions needed a common software base to provide a more streamlined design. Further, the basic man-machine interface—keyboard layout and rules of operation—remain unchanged for each implementation to facilitate user training.

The name of each of the three TRON segments denotes its intended application. I-TRON, where "I" stands for industrial,

TECHNOLOGY TO WATCH is a regular feature of *Electronics* aimed at providing readers with exclusive, in-depth reports from companies around the world on important technical innovations. It covers significant technology, processes, or developments incorporated in major new products. The reports also provide analyses of technical data, so that readers can assess the impact of new developments. Ken Sakamura, computer science professor at the University of Tokyo, conceived the TRON operating system described here.

is geared to engineers developing applications for embedded systems and features fast task dispatching.

B-TRON, geared to business users, boasts a bit-mapped display for use with such business graphics as pie charts and for work-station applications. Home, or H-TRON, will venture into a new area—environmental control in the home, office building, and factory of the future. It will include loosely coupled networks of separate I-TRON controllers and B-TRON consoles.

The TRON project originated with Sakamura's analysis of a study by the Japan Electronic Industry Development

Association. The Operating System Subcommittee of the group's Microcomputer Software Application Committee conducted a survey of microcomputer applications in Japanese industry in 1980 and 1981. As a result, the association compiled a list of users' microcomputer needs. A system, it recommended, should have the following characteristics:

- Real-time response, with task-switching times on the order of milliseconds.

1. Proto-TRON. A prototype 68-K I-TRON system has been implemented on a personal computer. A commercial version should hit the market next year.



- Operating-system software structured for easy incorporation (that is, in read-only memory) into larger systems.
- File-processing and data-communication functions.
- Flexible design so that improvements can be added or folded into current design.
- Uncomplicated operations and maintenance.

From this framework, which verified for Sakamura his theory of evolution for personal computers, the TRON project took shape. First, however, Sakamura formulated a stripped-down development plan.

His university research group started by developing the operating-system nucleus. This core component contained those operating-system software modules common to all three final TRONs. Dubbed the TRON chip nucleus, it comprised task management, memory management, synchronous communications functions, and interrupt-processing functions. Though a first-cut version, customers could use the TRON chip nucleus by itself as a primitive small-scale development system.

The project's second phase (complete for I-TRON, and in process for B- and H-TRON) was marked by the construction of command interpreters and file processors specific to each TRON version. These additions are unique for each segment.

The I-TRON segment consists of a real-time multitasking operating system for on-chip incorporation in embedded systems. Along with the TRON chip nucleus, it has file processing and a basic debugger.

The new software modules, the TRON nucleus peripherals, were burned into a separate ROM. (TRON is modular—the chip nucleus resides on one ROM, the peripherals on a second ROM.)

Multiphase project

To build B-TRON, the developers are enhancing an I-TRON with file management, expanded debugging functions, expanded input/output, display management, and command line interpreter. B-TRON supports windowing and parallel processing hookups.

One unique B-TRON feature is its ability to process Japanese. A basic dictionary facilitates the conversion of phonetic input to Japanese kanji characters; the system uses 16-bit character codes internally to handle the characters.

The software technology developed to cope with Orient-

tal-language processing could be a boon to Western-language-based computers as well. "These capabilities could greatly improve the efficiency of spelling checkers and pattern-recognition systems there," Sakamura notes.

The home portion of the TRON triad emphasizes the man-machine interface. Consequently, second-phase development for H-TRON will concentrate on connections to the outside world. The idea is to support a full range of those control functions that are likely to be used in environmental control.

Interfaces for communications, music, audio, and electrical-device switching will be designed. TRON will also support graphics. Because nonprogrammers are likely to use the system heavily, H-TRON's command-line interpreter will be superior to I-TRON's and B-TRON's.

Future phases

The thrust of the third and final TRON phase will be in hardware. The goal is to place the system on a 1-million-element VLSI CMOS chip containing a 32-bit central processing unit. TRON's developers are preparing supporting architecture in anticipation of the chip's realization in about three years.

Most important is the design of a standard bus called Tobus, to be used in conjunction with the VLSI TRON chip. Tobus has a standard 32-bit-wide data bus and address bus. Extended to 48 bits, the address bus will accommodate a large auxiliary memory, such as an optical disk. Stretched 64-bits wide, an extended data bus will facilitate high-speed transfer handling—ideal for image processing.

The system's designers envision a multitude of application-specific systems built from hybrid TRON architectures. Because of the commonality within its basic software, the various operating systems can be used as building blocks for future large-scale distributed-processing systems. TRON's strong communication functions will facilitate this sort of design, Sakamura says.

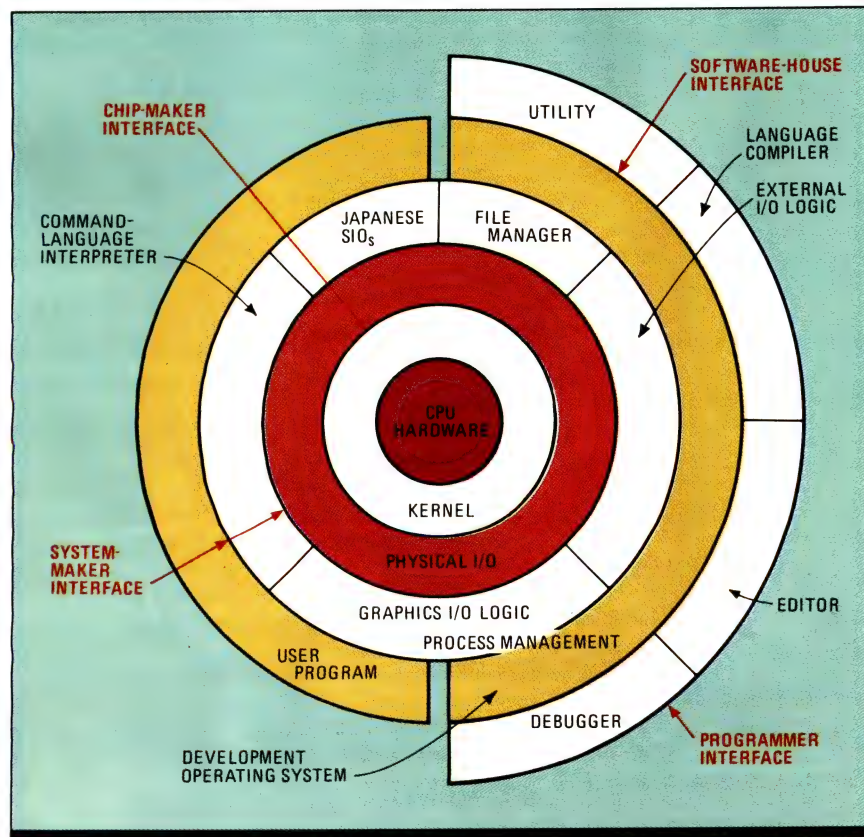
One such possibility is decentralized control for robotics.

A basic TRON chip could control robot joints, I-TRON could control spinal functions, and B-TRON could control the "brain." In addition, H-TRON could control overall communications, linking the robot and the home.

In the three years since its inception, the TRON project has received 100 million yen (equivalent to \$400,000). The bulk of the funding came through research grants from large manufacturers. Approximately 5% of the project's total cost came from Ministry of Education and University of Tokyo research funds.

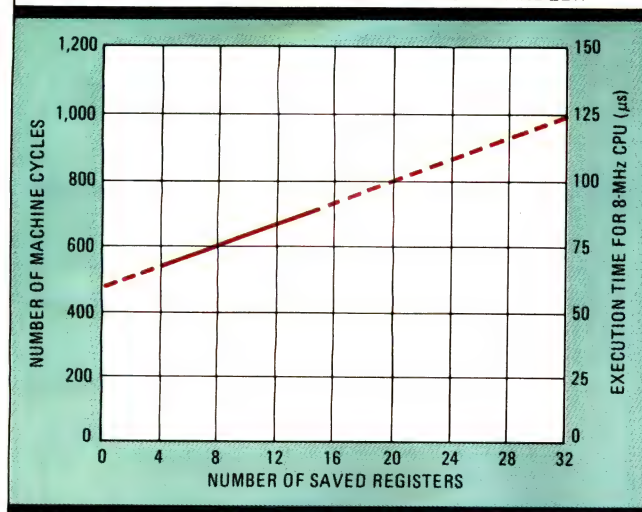
The money resulted in the construction of a personal computer-sized TRON prototype (Fig. 1), using a Motorola 68010 CPU. Sakamura expects a similar machine to be available commercially next summer for about \$1,200. Currently, I-TRON is working, with B-TRON to follow soon, on emulators consisting of Intel and Motorola CPUs.

Sakamura's research group has the instruction-set processor for the VLSI version of TRON under development. He expects it to take perhaps two more



2. Nucleus. TRON's real-time system architecture extends from CPU hardware to user-level application programs.

EXECUTION TIME OF RETURN-FROM-INTERRUPT HANDLER



3. Savings time. The time consumed by task redispach after interrupt handling increases with the number of registers that must be saved. To save eight registers, the system uses 612 machine cycles.

years before a commercial "micro-TRON chip" with 32-bit linear addressing is available. A larger-scale TRON chip with both 48-bit memory management, for use with laser disks, and additional memory on chip will follow a year or two later.

To date, TRON software has been developed only for Motorola 68000-type and Intel 8086-type CPUs. Additional chips have not been used because they are more difficult to buy in Japan and development systems are not readily available, says Sakamura. So that the TRON chips are not shunned for the same reason, he says that TRON development systems will become available at the same time as the TRON systems.

At NEC, TRON's launch licensee, Hiroshi Monden, assistant manager of the Microcomputer Products Division's system design department, says that his firm is officially implementing I-TRON. The Tokyo company will call the software RX116. It will be available for NEC's V20 through V50 processors; some form of RX116 will also be

available for the V60 processor. RX116 for the V20 and V30 processors was released this month.

Small code size and high speed are features of the product, says Monden. He claims that an RX116 with V20 processor runs an average of 1½ times faster than Intel's 8086-based RMX-86.

Though NEC is not working officially on B-TRON, its engineers are keeping abreast of its progress. Monden suspects that two competing manufacturers will announce prototypes this fall. NEC cannot move easily in this direction, he says, because its PC-9800 commands about 70% of Japan's 16-bit microcomputer market. Thus although a high-end B-TRON machine would be more functional than the PC-9800, the company would be competing against itself.

The company's series of PC-9800 machines includes a recently announced Intel 80286-based unit. This is a high-end machine, but it still does not provide the full set of functions possible with B-TRON. Though it might be possible to implement a subset of B-TRON on the PC-9800, it is not clear just how high the resulting performance would be, Monden says.

Some performance statistics are available on the prototype I-TRON package. That implementation, on a 68000 chip, requires 68-K bytes of memory. The system's task-management function code occupies approximately 3-K bytes. About 8-K bytes are needed to hold the operating system kernel.

The size of the task-control block will vary, depending on the number of registers to be saved. A 68000 has 15 registers, but considerable speed and memory savings result if the number saved are limited to eight. The task-control block occupies $56 + (4 \times R)$ bytes, where R is the number of registers to be saved at the task context switch. Thus the task-control block requires 116 bytes if all 15 registers are saved, 88 bytes for eight registers.

Task-switching speed

One of the bigger factors affecting real-time response is an operating system's task-switching speed. Total task-switching time is calculated as the number of machine cycles used by the interrupt handler.

The interrupt handler saves the 68000 registers, determines which interrupt occurred, and branches to the appropriate processing routine. Upon completion of that routine, it restores the registers and returns to the interrupted processing. Measured in clock cycles (exclusive of the processing time of the branched-to software itself), when eight registers are saved, total task-switching time is $(1,030 + 54A)$ machine clock cycles, where A is the number of tasks with a priority lower. With all 15 registers, the measure is $1,142 + 54A$. Sakamura claims that I-TRON's task-switching time is "one of the best among existing real-time operating systems."

A greatly simplified measure is the execution time of the return-from-interrupt handler. This routine restores the registers and returns to the main software branch at the conclusion of interrupt processing. Its execution time is $484 + (16 \times R)$ machine clock cycles. Thus for 15 registers, the number is 724 cycles, or 91 μs. With eight registers, the return-from-interrupt handler needs only 612 cycles, a speed saving of approximately 15%. Sakamura notes that performance data was obtained from the current TRON implementation. Fine tuning of future versions, he hopes, may further improve the system's performance.

As TRON progresses, Sakamura believes that it will be an open project. He expects that project results will eventually be published. A thousand TRONs will bloom, since anyone will be free to make use of the specifications of the architecture and operating system. □

PERFORMANCE OF V20/V30 I-TRON

Topic	RX116 (I-TRON)
Code size	8-K bytes
Timer resolution	1 ms
Context switch time	80 μs
Average time for system calls	250 μs (being measured)
Scheduling policy	Priority-based
Round robin	Possible
Resource creation or deletion	Dynamic
Definition of a routine executed at task completion	Normal, abnormal, forced
Clock operation	Periodic wake, delayed wake, wake at given time
Synchronization mechanism	Event flag, semaphore, mailbox
Exception handler	System call, CPU operation

HIGH-SPEED NETWORK BEATS MARKET LEADER'S PRICE

Startup offers more powerful system that transmits at 25 Mb/s, full duplex

Abrash newcomer in the world of high-speed networks hopes to reverse the notion that age and experience will triumph over youth and skill. Computer Network Technology Corp. (CNT) plans to deploy state-of-the-art technology to build a better, less costly product than the one from the company its principal founders left.

With its Lanlord high-speed networking system, the startup takes dead aim at the eight-year-old Hyperchannel network built by Network Systems Corp. Network Systems has been the leader in high-speed networking systems for linking supercomputers, mainframes, and lower-echelon machines and peripherals made by a variety of manufacturers (see related story, p. 36).

Lanlord's design relies on a carrier-sense multiple access with collision avoidance protocol and features full-duplex adapters, or system-access units (SAU), that attach to computers using standard television cable. Initial SAUs will house up to three 68000s, two 24- to 48-bit-wide 2901 bit-slice processors, and 256-K bytes of standard memory (expandable to 10 megabytes) to handle device-to-network protocol conversions. With that kind of horsepower, CNT claims its 25-Mb/s Lanlord will equal or better the message throughput of the half-duplex Hyperchannel (despite the latter's 50-Mb/s raw speed) but sell for about half the price.

Though Lanlord is not plug-compatible with Hyperchannel, it is system compatible. A product that plugged directly into the Hyperchannel cable could violate a Network Systems' patent, notes Eugene D. Misukanis, cofounder and executive vice president of CNT and a former Network Systems employee.

Friendly. Lanlord will run with any host software developed for Hyperchannel, including Network System's Netex; Massnet, from Masstor Systems Corp., Santa Clara, Calif.; and Hyper-link from Internet Systems Corp., Sunrise, Fla., which is a CNT joint-venture partner. "A Lanlord network could communicate with a Hyperchannel network through a host processor," Misukanis adds.

The company should complete beta-testing Lanlord this month at McDonnell Douglas Corp. and plans to ship its first production SAUs during the third quarter [*Electronics*, July 15, 1985,

p. 11]. Its initial offerings will include an SAU, to be available in August, that uses a CNT protocol to emulate Network System's Hyperchannel A220 adapter for connecting IBM Corp. mainframes, including the 43XX, 303X, and 370 lines, to a Lanlord net. A second Lanlord SAU, planned for September delivery, will handle a DR11W interface for connecting machines made by Digital Equipment Corp. on the same net.

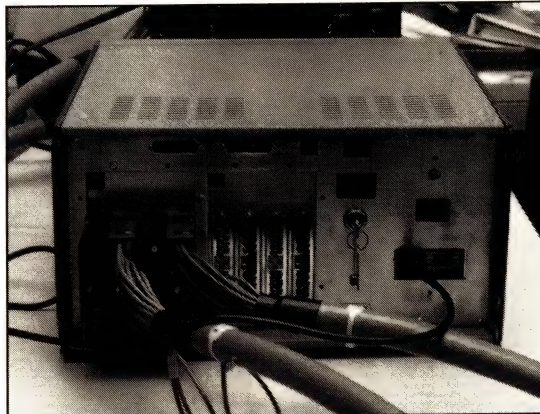
CNT will also address the IBM-only market with a SAU that is not compatible with the Hyperchannel system; this will also be available next month. Called the Channelink, it is designed as a replacement for IBM's 3088 channel-to-channel adapter for connecting IBM mainframes using IBM host software

such as JES3, ACF/VTAM, GRS and IMS-MSC.

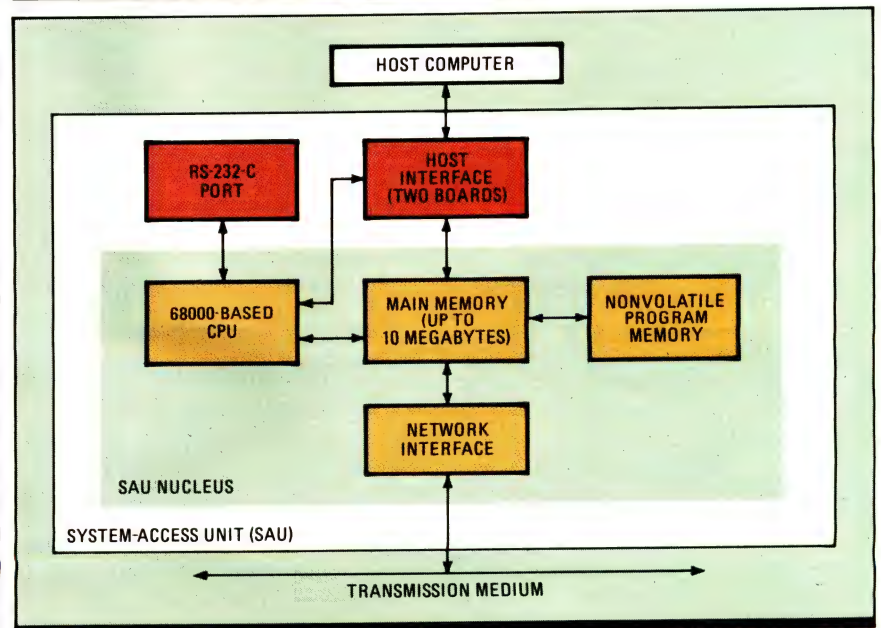
Each Lanlord SAU will sell for \$24,980, compared with Hyperchannel's typical \$40,000 to \$50,000 price per node, points out Robert A. Lutnicki, CNT vice president of marketing. Each Lanlord net will be able to link hosts 2,500 ft apart. A link adapter called Linklord, set for fourth-quarter availability, can tie together two or more Lanlord nets at 25 Mb/s, says Misukanis.

Also scheduled for delivery before year-end is a Linklord model that will allow use of a T-1 phone carrier (which operates at 1.54 Mb/s) to connect remote Lanlord nets. Final prices for the Linklord models and a planned Skylord unit, for handling satellite links, should fall in the \$25,000 to \$40,000 range, depending on the amount of memory required, says Misukanis. Skylord should go into production in the third quarter of 1986.

Also in the works are SAU versions that will attach to fiber-optic media. Because of



Nucleus. Computer Network Technology will have to modify only the computer interface (below) of its Lanlord system-access unit (left) for it to run on computers other than IBM's.



the SAU's modularity, producing units to interface to different computers will not be a major task, Misukanis indicates. Each SAU has a nucleus of four modules—the 68000-based CPU, main memory, nonvolatile program memory, and the network interface—which will remain the same for every SAU. Each SAU uses a VMEbus architecture.

A fifth module, the computer interface, will typically consist of two boards and will be the only portion of the SAU to require modification for each new host supported. The first board will require changes only in microcode; about 60% of the hardware on the second board will need modification depending on the host, says Misukanis.

The SAU cabinet measures 9.5 by 17 by 17 in. CNT will sell Lanlord to end users as well as to original-equipment manufacturers and valued-added resellers. Discounts for large quantity purchases will be available.

The initial release of Hyperchannel system-compatible Lanlord products will depend upon host-based software such as Netex to drive the SAUs. But by next year's first half, CNT plans a second 25-Mb/s release featuring Lanlord SAUs that will interface at the fourth, or transport, level of the International Organization for Standardization's model for open-systems interconnection.

At that time, CNT plans to introduce corresponding host-based software developed by itself or others. By placing responsibility for functions for the transport level and below on the SAU, CNT aims to reduce some of the processing burden now placed on the host when using packages such as Netex, Lutnicki explains.

A third Lanlord release, tentatively scheduled for next year's second half, will boost Lanlord's channel speed to 50 Mb/s.

—Wesley R. Iversen
Computer Network Technology Corp., 9440 Science Center Dr., New Hope, Minn. 55428. Phone (800) 638-8324 (in Minn., [612] 535-8111) [Circle reader service number 338]

DEPOSITION SYSTEM GROWS GaAs WAFERS

The SPI-MO CVD 1000 is a metal-organic, chemical-vapor-deposition system for growing epitaxial structures of gallium arsenide and related class III-V and II-VI compounds such as mercury cadmium. It is designed to work in atmospheric or low-pressure conditions.

With a capacity of 20 2-in. wafers or 12 3-in. wafers, the 1000 is fully automatic, offering totally programmable ramping control of all flows and temperature. Its thickness control is held to

$\pm 5\%$ and doping control to $\pm 10\%$, according to the manufacturer. The deposition system, which features a typical growth rate of $0.06 \mu\text{m}/\text{min}$, comes with one to six metal-organic sources and 1 to 10 gas lines. An average system sells for about \$275,000. Delivery takes six months.

Spire Corp., Patriots Park, Bedford, Mass. 01730. Phone (617) 275-6000 [Circle 359]

DIE BONDER BOOSTS HYBRID YIELD

The model 4000 eutectic die bonder increases yields of hybrid semiconductors, the manufacturer says. It features an optional hot nitrogen jet for spot heating bonding areas and leaving the rest of the substrate unaffected.

The unit scrubs dice with a $\pm 10^\circ$ rotary action. An optional linear scrubbing motion improves wetting on smaller die-bonding pads, the company says. Using



solid-state controls, the system keeps the substrate temperature controlled to 500°C ; it can adjust Collet temperature to 200°C . The model 4000 accepts various types of packages. An automatic indexer is optional. The basic unit sells for \$5,975. Delivery takes six to eight weeks.

Semiconductor Equipment Corp., Box 779, 5154 Goldman Ave., Moorpark, Calif. 93021. Phone (805) 529-2293 [Circle 360]

VECTOR MACHINE RUNS IN GIGAFLOPS RANGE

Two supercomputer vector processors, the models 1400 and 500, have processing speeds of up to 1.14 billion and 133 million floating-point operations/s, respectively. The model 1400 possesses 256 megabytes of main memory; the model 500 has 128 megabytes. Both supercomputers can use IBM Corp. Sys-

tem 370-compatible peripherals. Software for the pair of supercomputers is the Vector Processor/Application Development System, consisting of Fortran compilers and on-line program-development tools.

The model 500, which will sell for \$4.9 million to \$9.7 million, will be available in the fourth quarter of this year. The model 1400, planned for the second quarter of 1986, will sell for \$12.5 million to \$21.8 million.

Amdahl Corp., P.O. Box 470, Sunnyvale, Calif. 94086.

Phone (408) 746-6000 [Circle 340]

GOULD JUMPS INTO PARALLEL PROCESSING

A multiple-node processor system represents Gould's plunge into the world of parallel processing. Called Sci-Clone/32, the system uses Gould's Concept/32 minicomputers as independent parallel-processing nodes connected by a reflective memory system (RMS).

Sci-Clone/32 is a modular system, available with plug-in enhancements that come in increments of 0.5 million instructions per second up to 1.7 mips. A maximum system consists of a host computer, an eight-node RMS bus, and four parallel-processing units in each node, plus software—for a total of 30 mips of equivalent performance.

Gould designed Sci-Clone/32 for such real-time applications as flight simulation, signal processing, power-plant simulation, energy-management systems, and seismic data processing. The processor system, available in the first quarter of 1986, will sell for \$277,200 to \$1,377,000.

Gould Inc., Computer Systems Division, 6901 W. Sunrise Blvd., P.O. Box 9148, Fort Lauderdale, Fla. 33310.

Phone (305) 587-2900 [Circle 341]

REDUNDANCY KEEPS COMPUTER RUNNING

Redundant self-checking architecture promises data security in models 30 and 40 of Parallel Computer's 300 XR family of minicomputers. All the key components, including the CPU, memory, and integrated uninterruptible power supplies, are duplicated: if a component fails, its twin continues to work. Duplication on separate disk subsystems, automatic recovery from media failure, and end-to-end verification ensure data protection.

The 300 XR family has automatic fault detection and diagnosis. Users can replace modules while the system is running, the company says. The model 30 supports eight users, the model 40 sup-

ports up to 16 users. The system's maximum configuration consists of 8 megabytes of main memory and over 2 gigabytes of disk storage and supports 32 users. Ethernet is an option.

Model 30 sells for \$59,900, and model 40 sells for \$74,900. A five-year warranty for all repairs sells for \$9,000. The company offers discounts to value-added resellers.

Parallel Computers, 3004 Mission St., Santa Cruz, Calif. 95060.

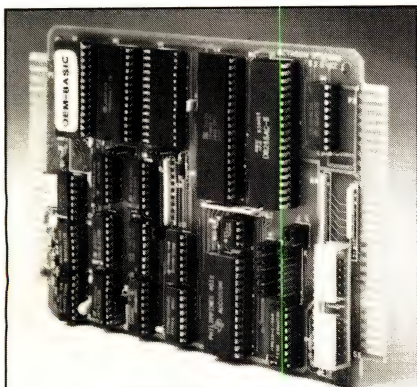
Phone (408) 429-1338

[Circle 342]

CONTROL COMPUTER HAS BUILT-IN BASIC

A single-board control computer based on a 4-MHz Z80A microprocessor features built-in Basic and a debug monitor, so users can combine the computer language with object code.

The SYS-3Z has its own EPROM programmer, 16-K bytes of EPROM, a bus-expansion port, an RS-232-C serial port, 8-K bytes of RAM, and 35 lines of analog and digital I/O. Because the SYS-3Z acts as its own development system, a user needs only a CRT and a +5-V power supply to write programs and subrou-



tines for storage in EPROM. The board sells for \$395 apiece. Delivery is from stock but can take up to two weeks.

Octagon Systems Corp., 6501 91st Ave., Westminster, Colo. 80030.

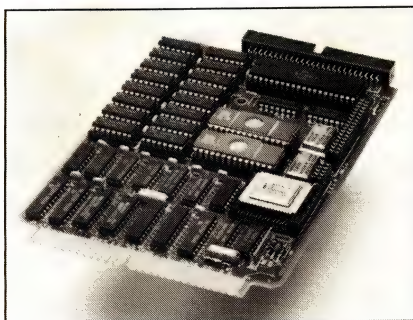
Phone (303) 426-8540

[Circle 368]

STD-BUS BOARD USES 16-BIT CPU

Based on Intel Corp.'s 8-MHz 80186 microprocessor, an STD-bus board-level computer has up to 512-K bytes of dynamic RAM and 64-K bytes of ROM. An additional 128-K bytes of memory is optional.

All on-board operations take advantage of the CPU's 16-bit power but leave the 8-bit bus undisturbed. The board, which includes software to link it with a personal computer or another RS-232-C system, has two 8-bit parallel ports in addition to the RS-232-C interface. A



standard 128-K configuration sells for \$550 and is available now.

Cubit, 190 S. Whisman Rd., Mountain View, Calif. 94041.

Phone (415) 962-8237

[Circle 369]

COMPUTER BOARD HAS DMA CONTROLLER

Designed for applications in robotic and process control, the CPU-4 processor-board series works either in systems with disk storage or in diskless systems where the operating system and application program are permanently stored in memory chips on the board.

Using a 12.5-MHz 68010 microprocessor, the board accesses local static RAM without wait states. The SRAM can be either 32-K or 128-K bytes. An on-board direct-memory-access controller transfers data without program control between local RAM or I/O chips and the VMEbus.

The board, with a base price of \$2,005, also has eight EPROM sockets for up to 512-K bytes of program storage, a serial interface with multiple protocols, and a real-time clock with battery backup. The price also includes monitor and debug-firmware for the CPU.

Force Computers Inc., 727 University Ave., Los Gatos, Calif. 95030.

Phone (408) 354-3410

[Circle 367]

SINGLE SUPPLY POWERS EEPROM

A 16-by-16-bit EEPROM chip for data storage or timing works with industrial controllers and data-communications equipment. The M9306 serial-access memory includes an on-chip programming voltage generator so that a single +5-V source can supply the power. Standby current is 3 mA; operating current is 10 mA with a clock frequency of 250 kHz. It retains programmed information for up to 10 years.

The M9306 EEPROM is available in either a plastic or a ceramic 8-pin package. In quantities of 1,000, it sells for \$3 per unit.

SGS Semiconductor Corp., 1000 E. Bell Rd., Phoenix, Ariz. 85022.

Phone (602) 867-6100

[Circle 354]

CONTROLLER CHIPS SAVE BOARD SPACE

Most hard-disk controllers require at least 50 ICs in their designs. But a two-chip set can cut that figure by 80%.

The set consists of the μ PD7261 controller and the μ PD9306 interface chip. The controller simplifies the software drivers; the interface handles the circuitry as well as provides digital phase-locked loop and precompensation. The set, which supports both the ST-506 and storage-module-drive formats, acts as an interface for a hard disk and CPU.

The controller chip comes in a 40-pin DIP; the interface chip comes in a 28-pin DIP. In large quantities, the set sells for under \$25. Samples of the chip are available immediately.

NEC Electronics Inc., P.O. Box 7241, Mountain View, Calif. 94039.

Phone (415) 960-6000

[Circle 355]

MICROCOMPUTERS RUN AT 12 MHz

Designers can develop full-speed prototypes with two 12-MHz versions of the 8751H 8-bit microcomputer. The two versions have either 4- or 8-K bytes of EPROM built into the chip for easier programming.

The manufacturer claims the parts can be programmed 15 times faster than competitive parts, because of an adaptive programming process. The chips come with four 8-bit ports, 32 I/O lines, and a full-duplex serial channel. They can access up to 64-K bytes of program memory and the identical amount of data memory, each located at different addresses.

The 8-K-byte version, the Am9761AH, sells for \$73.70 each in 100-piece quantities. The 4-K-byte version, called 8751H-12MHz, sells for \$63 each in the same quantities.

Advanced Micro Devices Inc., P.O. Box 3453, Sunnyvale, Calif. 94088.

Phone (408) 732-2400

[Circle 356]

ALGORITHM SPEEDS RAY TRACING

Ray tracing of images used to be slow and laborious. Now a proprietary algorithm speeds the process—the manufacturer of Visual:Genisys says the software produces images in constant time, independent of the number of objects.

The drawing time is based only on resolution, not on the number of objects or their visual complexity. Sample applications for ray tracing include architectural-shadow analysis, manufacturing layout, animation, and mechanical-parts fabrication, for which the process offers

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Engineers - Save precious time by eliminating a cumbersome series of software instructions.

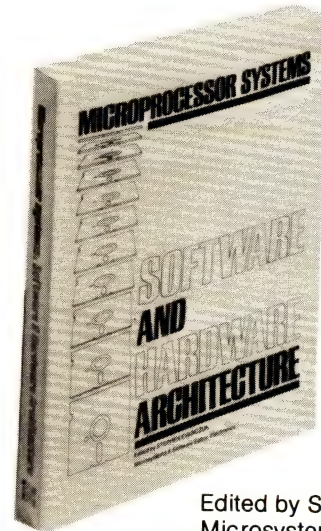
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Circle 64 on reader

full realism with rendering of multiple light sources, transparent images, and reflective surfaces.

Running in C programming language, Visual:Genisys has a subroutine-library interface for integration with three-dimensional data-generating applications. It will be available for the Digital Equipment Corp. VAX and for Pyramid computers running under Unix. Configurations for other Unix-based computers are in the works. Depending on system configuration, the end-user price will range from \$10,000 to \$75,000.

Visual Engineering Inc., 2680 N. First St., Suite 200, San Jose, Calif. 95134.

Phone (408) 945-9055 [Circle 346]

SYSTEM ADDRESSES 16 MEGABYTES

The iRMI 286 operating system has real-time processor management for time-critical applications and can address 16 megabytes of memory. It is suited for memory-intensive applications such as simulations and large private-branch-exchange systems, its maker says. Designed for systems based on the 80286 microprocessor, the iRMX 286 release 1.0 preserves the user's investment in the widely used iRMX 86 operating system, because a user can adapt code developed on it to iRMX 286 by recompiling the application source code.

The user can store the iRMX 286 operating system in PROMs and tailor it to applications. For example, I/O device-driver routines can be added or deleted from the operating-system configuration, depending on the need for special peripherals. The operating system supports the iAPX 80287 numeric processor extension for floating-point arithmetic.

Available now, the iRMX 286 is licensed to original-equipment manufacturers for a \$7,500 fee. Development-system support is also available.

Intel Corp., Literature Department W-232, 3065 Bowers Ave., Santa Clara, Calif. 95051 [Circle 347]

MODULE IMPLEMENTS JUST-IN-TIME CONCEPT

A Just-In-Time module is the latest to be added to Micro-MRP Inc.'s manufacturing-resource-planning software for IBM Corp. computers. Priced at \$4,000, the module is designed to optimize manufacturing efficiency by scheduling parts and planning labor resources on products planned for shipment.

Just-In-Time is based on the Signal system logic used by Toshiba Corp. With it, companies can plan material acquisition and schedule labor and production only as certain products are needed;

thus they can reduce inventory costs, optimize labor expenditures, and increase the efficiency of production schedules, the manufacturer says.

Micro-MRP Inc., 1065 E. Hillsdale Blvd., Foster City, Calif. 94404.

Phone (415) 345-6000 [Circle 348]

NEW MODE BOOSTS DRACULA'S SPEED

A true hierarchical layout-verification mode for any size VLSI circuit boosts the speed of ECAD Inc.'s popular Dracula engineering and computer-aided design software. On a typical 100,000-transistor circuit, Dracula III (in hierarchical mode) will verify a chip design 14 times faster than the earlier version, Dracula II, in flat-mode verification.

In hierarchical mode, Dracula III isolates each cell and verifies its structure only once for fast checking. The software is especially efficient with standard-cell, building-block, structural, memory, and microprocessor designs, the company says. It also completely checks the circuit layout.

Dracula III will run on a number of computers and work stations. The VAX-11/730 version sells for \$88,000. The VAX 8600 version sells for \$205,000. The software will be available for delivery sometime in September.

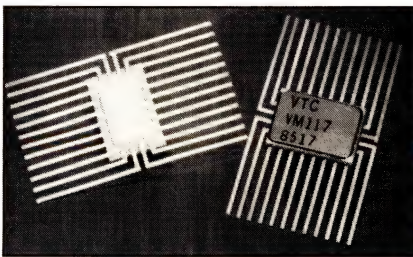
ECAD Inc., 2455 Augustine Dr., Santa Clara, Calif. 95054.

Phone (408) 727-0264 [Circle 349]

PREAMP PUTS OUT 33% LESS NOISE

Aimed at makers of 3½- and 5¼-in. hard-disk drives, the VM117 family of bipolar read/write preamplifiers uses center-tapped ferrite recording heads.

The preamps emit 33% less noise for



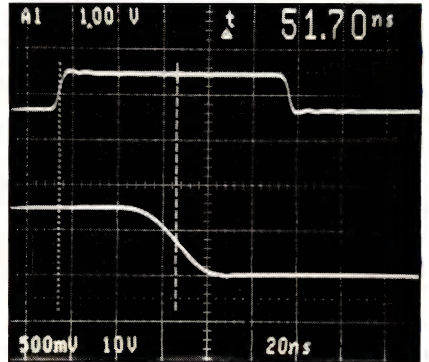
data signals in the read data path and stable operation makes ferrite beads in both modes obsolete. They operate on +5- and +12-V power supplies and come in two-, four-, and six-channel versions. Available in a variety of package types, the two-channel version sell for about \$5.20 each in lots of 1,000.

VTC Inc., Microcircuits Division, 2800 E. Old Shakopee Rd., Minneapolis, Minn. 55420. Phone (800) 352-6789 or (612) 853-4342 [Circle 363]

MODULATORS HAVE 50-ns DELAYS

The UC3825 series of high-frequency pulse-width modulators has a 50-ns propagation delay and an 8-MHz bandwidth-error amplifier with a slew rate of 12 V/μs.

The devices include protection circuitry consisting of a current-limit comparator, a TTL-compatible shut-down port, and a soft-start pin that can double as a maximum-duty-cycle clamp. Logic is fully latched, providing jitter-free operation, the company says, and an under-



voltage lockout section with 600 mV of hysteresis ensures clean startup.

The modulators come in three versions that differ by temperature grade. All have dual high-speed totem-pole outputs that can source and sink 1.5 A from highly capacitive loads. Housed in 16-pin plastic or ceramic packages, they range in price from \$3.40 each to \$11.40 each in 1,000-unit quantities.

Unitrode Integrated Circuits Corp., Linear Integrated Circuits Division, 7 Continental Blvd., Merrimack, N.H. 03054.

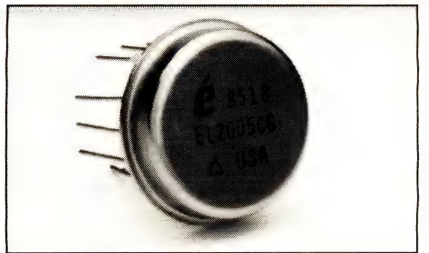
Phone (603) 424-2410 [Circle 361]

FAST BUFFER BOASTS HIGH RESISTANCE

Its 1,000-GΩ input resistance makes a high-speed FET input amplifier/buffer useful in sample and hold circuits.

Pin-compatible with industry standard buffer/amplifiers, the EL2005 boasts a fast 1,500-V/μs slew rate. The device, available in both military- and commercial-grade versions, comes standard in a TO-8 metal-can package but can be ordered in leadless chip carriers.

The military model, reliable in tem-



peratures ranging from -25°C to +85°C, costs \$44.23 in lots of 100; its commercial counterpart, the EL2005C, sells for \$20 each in like quantities. Delivery is from stock.

Elantec Inc., 1996 Tarob Court, Milpitas, Calif. 95035.

Phone (408) 945-1323

[Circle 362]

GENERIC LIBRARY BUILDS 3-MICRON ICs

A generic cell-design library, billed as foundry-independent, addresses the needs of systems designers who are replacing pc boards with large-scale, 3-μm CMOS circuits. The manufacturer says many of the leading foundries can produce Genlib 3000 designs, which are fully TTL-compatible. The library is compatible with Valid, CAE Systems/Tektronix, and Via work stations.

Customers can have the library, including all computer-aided-design support and a physical cell-layout data base, under any of four different licensing plans. Under the first plan, the manufacturer produces a complete turnkey design to the customer's specifications; the second and third plans give customer greater control over the design process. With the fourth plan, the customer does the complete design, through physical layout, using the manufacturer as a consultant only.

Pricing ranges from \$5,000 to \$30,000. Source III Inc., 4320 Stevens Creek Blvd., Suite 195, San Jose, Calif. 95129. Phone (408) 241-8871

[Circle 358]

SILICON COMPILERS AID CMOS DESIGN

Two silicon compilers, the VSYC2901 data-path compiler and the Logic Compiler, use an advanced 2-μm double-metal CMOS process.

Engineers can enter logic descriptions into the Logic Compiler through its schematic editor, resulting in reduced design time, the manufacturer says. Through this interface, engineers have access to flip-flops, counters, latches, gates, multiplexers, decoders, and other elements. The compiler can also generate cell blocks for use with other silicon compilers as well as complete chips.

The VSYC2901 builds on the architecture of Advanced Micro Devices' Am2901 bit-slice microprocessor. This allows users to translate board-level 2901-based designs to semicustom chips with minimal effort, the company says. Pricing of the compiler, which will be available in November, is not set.

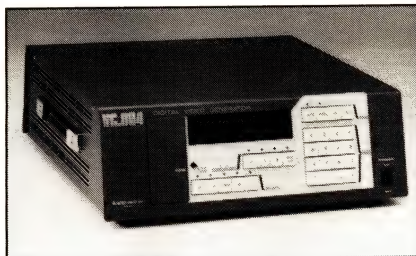
VLSI Technology Inc., 1109 McKay Dr., San Jose, Calif., 95131.

Phone (408) 942-1810

[Circle 357]

GENERATOR TESTS COLOR MONITORS

A programmable video-signal generator that tests both color and monochrome video monitors operates at horizontal scan rates up to 99 kHz and dot-clock frequencies from 4.38 to 50 MHz. The VG-804 has both analog and TTL outputs for connection to the monitor under test and offers independent timing and dot-clock controls. The user can program timing and pattern parameters from the front panel or burn the information into PROM as well as program individual characters. The instrument displays an invert key and top-left-hand-corner marker.



Available in 30 days after receipt of order, the VG-804 sells for \$5,700.

Test and Measurement Systems Inc., 349 Cobalt Way, Suite 301, Sunnyvale, Calif. 94086. Phone (408) 720-8877

[Circle 386]

INTERFACE LINKS HOST TO 15 PLOTTERS

With the RG interface, any personal computer with an RS-232-C port can control up to 15 peripherals on the IEEE-488 bus, including plotters, printers, disk drives, and data-acquisition and control systems. When the IEEE-488 peripheral operates in the transparent mode, it will look like an RS-232-C peripheral to the computer.

Available immediately from stock with case, power supply, and standard IEEE-488 and RS-232-C connectors, the RG controller sells for \$495.

Connecticut Microcomputer Inc., P.O. Box 186, Brookfield, Conn. 06804.

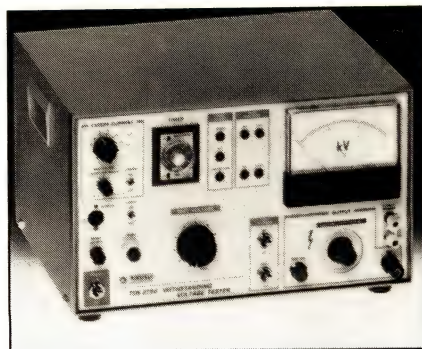
Phone (203) 354-9395

[Circle 387]

TESTERS MEASURE CURRENT LEAKS

A family of Hipot Testers measures current leaks between chassis and electronics as well as tests for opens, shorts, and arcing. The testers have a window detector, which recognizes when components are open and when test lead connections are poor.

The testers check safety specifications as set by the Underwriters Laboratories and the Canadian Standards Association. The family includes 0- to 5-kV and



0- to 10-kV models in both ac and dc versions.

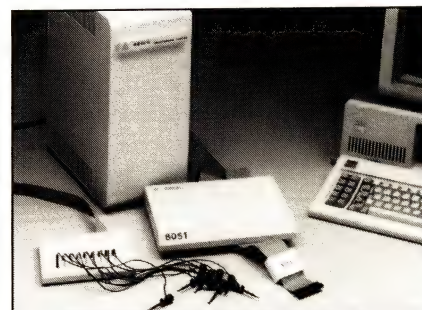
The testers have built-in timers with manual or 2- to 60-s settings, manually set current limits, and a current monitor output for connection to an external amplifier or multimeter. Available now, the instruments sell for \$655 to \$2,280.

Kikusui International Corp., 17819 S. Figueroa St., Gardena, Calif. 90248

[Circle 366]

TRACING IMPROVES DEVELOPMENT SYSTEM

Users can trace up to 4,096 events with the 4-K Deep Trace enhancement to the Ez-Pro 2.1 personal-computer-based development system. With Deep Trace, users can monitor lines and evaluate conditions during selected clock cycles. A complex triggering function permits flexible control of software testing.



Ez-Pro supports 65 different microprocessors—both 8- and 16-bit—for target systems. It connects to the IBM Corp. family of personal computers with a serial interface. The base price for the system, including 4-K Deep Trace, is \$8,665. Delivery is from stock.

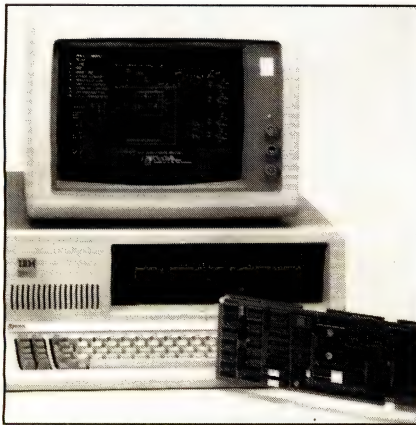
American Automation, 14731 Franklin Ave., Tustin, Calif. 92680.

Phone (714) 731-1661

[Circle 365]

BOARD DRAWS 20,000 VECTORS/S

The PG-1280 graphics controller board draws up to 20,000 vectors/s and supports a display resolution of 1,280 by 960 pixels by 8 bits for such high-density applications as architectural drawings. Its raster-dump direct-memory-access port transfers complete images,



such as Landsat photos, to the screen in under 1 s. Because it supports a complete emulation of the IBM Corp. color-graphics adapter, it can run popular programs such as 1-2-3 and Flight Simulator on the same screen that it uses for the high-resolution graphics.

The PG-1280 sells for \$4,995, with shipments scheduled for November. The PG-640, a graphics controller board with a resolution of 640 by 480 pixels by 8 bits, is available now, for \$2,495. The company offers volume discounts. Matrox Electronics Systems Ltd., 1055 St. Regis Blvd., Dorval, Quebec, Canada H9P 2T4. Phone (514) 685-2630 [Circle 352]

CARD ADDRESSES 1,024 BY 1,024 PIXELS

The Pepe graphics board set draws pixels in a fast 60 ns; third-party-software beta tests have validated speeds of over 60,000 400-pixel lines/s, the manufacturer says. Pepe also features an on-board character generator that supports 128 characters per line and 64 lines per page, with a display of 80 characters by 64 lines. Resolution is 1,024 by 1,024 pixels, with a 60-Hz noninterlaced video output.

The card comes in six frame-buffer configurations, including 12 bitplanes with 4,096 colors. Prices range from \$2,495 to \$4,495, depending on configuration. A 19-in. color monitor is also available, at \$3,495. Deliveries will begin in August.

Vectrix Corp., 2606 Branchwood Dr., Greensboro, N.C. 27408. Phone (919) 288-0520 [Circle 353]

SLIP-IN MODULE GIVES MODEM LONGER LIFE

A user-removable module holds the firmware for the Professional 2400 modem, simplifying updates and repairs to the 2,400-b/s unit. The module, which measures 5½ by 1¼ by ½ in., slips in and out of the modem's rear panel without disassembly.

Assembled using surface-mount technology, the Professional 2400 has optional feature modules that provide security password protection, a variety of protocols including X.25, and additional International Telegraph and Telephone Consultative Committee protocol compatibilities for international communications. Value-added resellers buying in volume can order customized modules.

The user controls operating mode and speed from the keyboard. The system displays its status in words rather than in symbols. Prices for the Professional 2400 are available on request.

Novation Inc., 20409 Prairie St., Chatsworth, Calif. 91311.

Phone (213) 996-5060 [Circle 350]

VOICE, DATA COEXIST ON SINGLE LINE

The Fastalk 300 line of modems lets users hear a voice on line during a data call, thanks to a built-in speaker with volume control. Because of the speaker, the user can switch between voice and data without having to change modes. All three models—the 300, the 1200, and the 1200 PC, a plug-in modem card—offer call-progress monitoring of dial-tone, busy, ring, and connect signals.

SignOn communications software comes with each modem. It features a learn mode that logs on, retrieves data, and signs off; it also incorporates auto-start for unattended operation.

Fastalk modems fit underneath a standard telephone base and work with any terminal having an RS-232-C interface. Resale prices are \$345 for the model 300 and \$525 for the models 1200 and 1200 PC.

Universal Data Systems Inc., 5000 Bradford Dr., Huntsville, Ala. 35805.

Phone (205) 837-8100 [Circle 351]

COMPUTER ENHANCES DATA-CONTROL UNIT

System 10 users can add the manufacturer's Industrial Personal Computer, which offers an optional internal solid-state memory disk, to their data-acquisition and control system. With the optional machine, System 10 owners get such useful data-processing capabilities as Basic programming, color graphics, and data storage.

Replacing one of the two standard floppy-disk drives, the solid-state disk's 128-K bytes of write-protected memory contains the operating system. Thus the computer can be booted without magnetic disks, which are easily damaged in the industrial environment. The internal disk also offers a battery-backed file memory of 224-K bytes.

Identical in size to the model 10K1 Datapac terminal, the Industrial Personal Computer can be mounted in any 19-in. rack; it has 256-K bytes of RAM and comes with an RS-232-C serial port and a Centronics parallel printer port. The company provides eight colors for graphics and software that time-plots data in real time. Available now, the computer is priced at \$2,395.

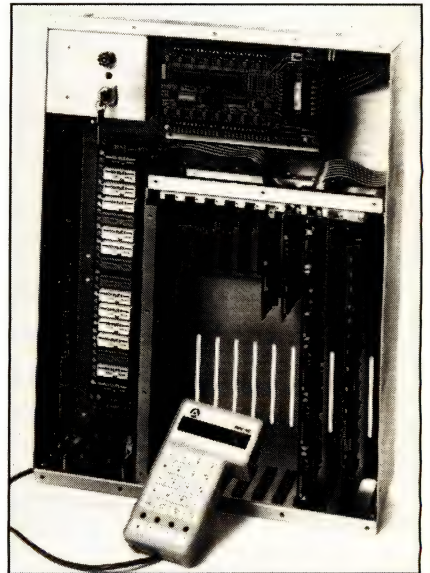
Daytronic Corp., 2589 Corporate Pl., Miamisburg, Ohio 45342.

Phone (513) 866-3300 [Circle 343]

COMPUTER RUNS IN DIRT AND DAMPNES

Designed to mount in a standard National Equipment Manufacturers Association cabinet, the RPC-50 is an industrial microcomputer compatible with the IBM Corp. Personal Computer. External surfaces are built of heavy-gauge metal and sealed. With an optional heat exchanger, the RPC-50 can be completely sealed in a watertight cabinet.

The computer is designed to operate in harsh environments—in the presence of dirt, vibration, radio-frequency fields, and fluctuating or noisy power lines—and within a temperature range of 0° to



+55°C. Typical applications include control of ovens, electroplating systems, and vacuum-deposition equipment.

Mounting facilities for I/O, solid-state relays, and multiplexers are inside the cabinet yet isolated from the computer. Seven full-size expansion slots are available. Users can develop applications directly on the RPC-50—even program EPROMs in place, the manufacturer says. The RPC-50 costs under \$2,000 in large quantities.

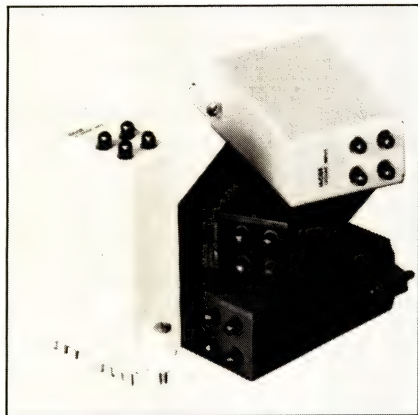
Amdex Corp., 16 Woodhaven Dr., Andover, Mass. 01810.

Phone (617) 470-0561 [Circle 345]

QUAD I/O MODULES SHRUG OFF NOISE

Four-line I/O modules, color-coded by function, suit series-operations systems that use input modules to monitor load status. Transient-noise immunity is above 3,000 V, thanks to an internal snubber network for protection from on-line voltage transients.

Modules are available for 5-, 15-, and



24-V dc logic systems, and all come in industry-standard plug-in enclosures. The manufacturer also has mounting boards that accommodate six or eight of the quad I/O modules.

The modules carry a price tag of \$24 each in 500-piece quantities. The mounting boards are priced at \$75 each in 100-piece quantities.

AMF Inc., Potter & Brumfield Division, 200 S. Richland Creek Dr., Princeton, Ind. 47671. Phone (812) 386-2183 [Circle 344]

IC TEST SYSTEM WORKS IN REAL TIME

Simple, understandable reporting is a primary objective of Intersect 10, a burn-in and test system that conditions and tests volatile and nonvolatile memories and accommodates dynamic or static devices. It can also program EE-PROMs. Programmed in Bits Basic, Intersect 10 delivers real-time reports on current yield levels and trends in production performance and quality.

The reporting function also presents bit maps of passed and failed cells for every device under test. Then automatic system verification ensures rapid identification of error conditions that might compromise test results.

Utilities are included in the Intersect 10 system software that reduce programming tasks. Thus it has an algorithm for pattern generation, and the user can select any of 16 programmed timing sets on the fly. The user can change conditions—such as voltages in a pattern-analysis system, or burn-in temperatures—without writing a sepa-

rate program for each alteration. Address scrambling is a standard feature; a test-vector memory is optional.

Users can also link Intersect 10 with a network. As part of a net, it sends real-time data to management information systems, to a host computer, or to an automatic unloader-sorter machine.

The price of a typical Intersect 10 system, with a device capacity of 3,600 16-pin ICs and three pattern generators, is around \$400,000; configuration is possible for 7,200 16-pin devices. Delivery takes approximately 120 days after receipt of order and approved system specifications.

Reliability Inc., P.O. Box 218370, Houston, Texas 77218.

Phone (713) 492-0550 [Circle 373]

CAD HELPS IN TEST-HEAD DESIGN

With its interactive graphics, the Pen-Entry Test Head Programmer saves up to 70% of the labor and time required for constructing bed-of-nails test heads, the manufacturer says. This computer-aided-design system generates numerical-control tapes to drill and wire the test head on automatic machinery. It also plots a map of the test head that identifies all nodes wired to a specific test-block-interface pin. This permits nodes to be quickly located for both fixture wiring and post-test rework.

In addition to node mapping, the system's standard functions include test-probe transfer, sequential numbering of test points, renumbering of nodes, and repetition of certain patterns.

The system creates the test-head geometry directly from the original pcb-board drill tape. Hole patterns are displayed automatically on the system's CRT; then the engineer uses a light pen to select or delete points. The engineer can add or change probe numbers using a mouse to reference locations on the screen; afterward, they are automatically annotated with revised probe-transfer plots. For companies that annotate by hand, the changes can be printed on Mylar, then overlaid on the schematic and photographed for reprinting.

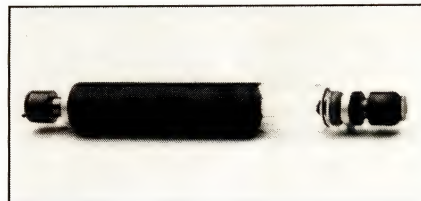
A Pen-Entry Test Head Programmer system consists of a 15-in. CRT, control center with keyboard, desk console, CPU with 136-K bytes of main memory, an 8-in. floppy-disk drive, paper-tape reader and punch, and an 11-by-17-in. flatbed plotter. Software is available for systems by a range of companies. Prices start at \$39,500, and delivery takes four to six weeks.

Wire Graphics Inc., 215B Central Ave., Farmingdale, N.Y. 11735.

Phone (516) 293-1525 [Circle 374]

HeNe LASER TAKES THE HEAT

This helium-neon laser copes with the problems of gas volume, heat dissipation, and current density at the cathode that usually plague lasers of this size. The 5/8-in.-diameter laser's proprietary design features a Kovar housing, which reduces heat problems. Its symmetrical cathode reduces current density. The



randomly polarized minimum output is 0.5 mW at 632.8 nm.

Current operation is low—3 mA—for longer battery life. Root-mean-square optical noise is held to under 0.4%. The HeNe laser is 5 in. long, and the 0.46-mm-diameter beam has a divergence of 1.7 millirad.

The company builds the laser with its zero-leak hard seals throughout. It is suitable for rugged field applications, including laser sights for weapons, co-linear points for infrared lasers, and portable construction instruments. Prices and delivery information were unavailable at press time.

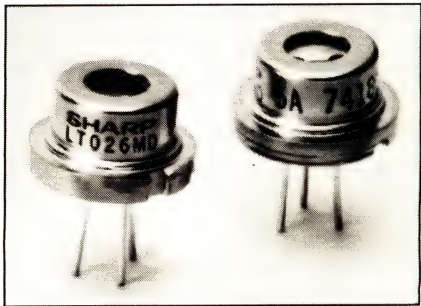
Melles Griot Laser Products, 435 S. Pacific St., San Marcos, Calif. 92069.

Phone (619) 744-7060 [Circle 370]

LASERS ARE BUILT ON V-CHANNEL SUBSTRATE

Using its V-channeled substrate inner stripe (VSIS) diode structure, Sharp Electronics has constructed two laser diodes—one with a visible beam and the other with a wavelength of 750 nm.

The visible-beam diode, the LTO26MD (pictured) emits 5 mW at an oscillation wavelength of 780 nm and is intended for use in a laser-beam printer. Sharp's VSIS technology provides precise control of the active substrate depth and V-channel width. This gives the diode an astigmatic distance of less than 10 μ m. It has a low threshold current and a



mean time before failure of better than 200,000 h at 25°C. It's easily coupled to lens systems.

The second diode, a gallium-aluminum arsenide device called the LTO30MD, has a short (750 nm) oscillation wavelength, giving it increased performance and sensitivity over the popularly used 780-nm diodes. This GaAlAs laser boasts a low threshold current and a signal-to-noise ratio of over 60 dB.

As an example of the diode's increased sensitivity, the company claims that bar-code readers employing the device could read more colors. Prices and delivery schedules were unavailable at press time.

Sharp Electronics Corp., Electronic Components Division, 10 Sharp Plaza, Paramus, N.J. 07652.

Phone (201) 599-3750

[Circle 371]

GaAlAs LASER DIODE PUTS OUT UP TO 50 mW

A multiheterojunction gallium-aluminum arsenide laser diode emits 50 mW, continuous wave. It is fabricated with metal-organic chemical-vapor deposition and housed in a fiber-stub package. The SDL-2410-H7's 0.3-numerical-aperture fiber stub, which has a 100- μ m-core, acts as an effective mode mixer and produces a symmetrical beam with a uniform intensity profile.

The company says the multiple quantum-well active-layer structure provides the high output power and low-threshold, highly efficient operation. Spectra suggests that the circular radiation pattern provided by an emitting region—consisting of 10 closely coupled, gain-guided, active stripes—is ideal for such applications as illumination, point-to-point communications, machine vision, range finding, and optical excitation.

The laser diode comes in an 8-pin TO-3 package.

Spectra Diode Labs, 3333 N. First St., San Jose, Calif. 95134.

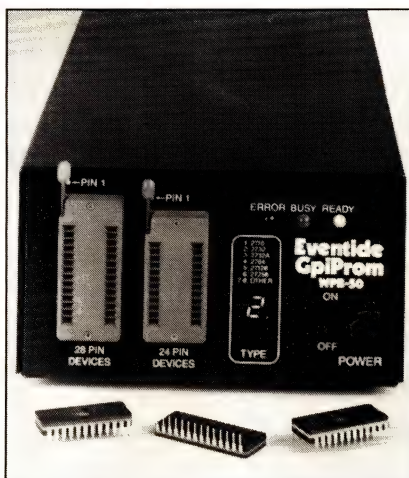
Phone (408) 946-3438

[Circle 372]

PROM BURNER USES IEEE-488 INTERFACE

Most PROM programmers operate with RS-232-C interfaces, but Eventide's programmer for Hewlett-Packard Co. computers performs on the IEEE-488 interface bus. The company says that users of HP computers with an IEEE-488 interface have had problems with RS-232-C because of the conversions required.

Called GpiPROM, the programmer burns in chips ranging in size from 16-K to 256-K, including 2716-, 2732-, 2764-, 27128-, and 27256-compatible parts. GpiPROM makes use of intelligent pro-



gramming algorithms for those chips that support them.

Priced at \$995, the programmer is available from stock.

Eventide Inc., 1 Alsan Way, Little Ferry, N.J. 07643.

Phone (201) 641-1200

[Circle 375]

SYSTEM PROGRAMS AND TESTS PROMs

Incorporating both testing and burn-in functions, the Omni ATE handles over 750 different EPROMs, EEPROMs, bipolar PROMs, programmable logic arrays, integrated fuse logic, and single-chip microcontrollers, thanks to software-configured pin drivers at each pin location. The system includes a full-screen parameter editor. Thus the user can modify any of the 15,000 ac and dc test and programming parameters, such as the program pulse width, the maximum current applied by the programming supply, and the voltage levels during standby, read, and programming modes.

The user can also modify a number of operational test limits, such as the maximum allowed read current, minimum voltage value for a TTL-high output, maximum voltage value for a TTL-low output, and the high and low margins of



the collector-supply current.

Available three to four weeks after ordering, the Omni ATE sells for \$8,650. Oliver Advanced Engineering Inc., 676 W. Wilson Ave., Glendale, Calif. 91203. Phone (818) 240-0080

[Circle 376]

FAST LOGIC ARRAY REPLACES ECL CHIPS

A maximum input-to-output delay time of 6 ns characterizes the PL106P8 programmable logic array. It is targeted as a user-programmable replacement for multiple discrete ECL chips in high-performance systems. The PL106P8, which is compatible with 10-KH ECL devices, is fabricated in the manufacturer's Oxiss oxide-isolated bipolar process. It uses titanium-tungsten fuse links to implement the programmable features.

The PL106P8 accepts 16 inputs to produce eight outputs. It is supported by the company's Plan software, which aids designers in device selection and development of the fuse-link pattern. The PLA has 2,048 fuses; output polarity is user-programmable.

In quantities of 100, the PL106P8 in a 24-pin ceramic DIP sells for \$19.85. Production quantities will be available in August.

National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, Calif. 95051. Phone (408) 721-5000

[Circle 381]

LINEAR ARRAYS BUILD CHIPS QUICKLY

The Quickchip analog-array family has two new members—Quickchip 2 and a smaller version, the 2S. The arrays, fabricated in the manufacturer's Super High 3 bipolar process, suit such applications as pulse generators, phase-locked loops, voltage-controlled oscillators, and a buffer amplifier with a bandwidth of 1.0 GHz. The line is also useful for analog switches and clock recovery circuits that require high speed.

The Quickchip 2 and 2S ICs offer the designer three different npn transistor sizes with peak frequency response at different operating currents. All three sizes have breakdown voltages exceeding 15 V. The npn transistors have a typical current-gain bandwidth frequency of 6.5 GHz; the pnp transistors have a typical bandwidth frequency of 50 MHz. Collector capacitances range from 0.20 pF to 1.26 pF.

The chips accommodate custom thin-film Nichrome resistors, which have values from 5 Ω to 10 k Ω . The Nichrome resistors are laser-trimmable to tolerances as tight as $\pm 0.01\%$.

Quickchip components are pre-designed, and detailed device models are

provided for Spice simulation. The manufacturer can fabricate wafers within three weeks of receipt of approved layout. Prices start at \$17,000 for prototype wafers or packages. Options and nonrecurring engineering charges will vary the price.

Tektronix Inc., P.O. Box 500, Beaverton, Ore. 97077.

Phone (503) 644-0161 [Circle 379]

SINGLE-MASK ARRAYS CUT DESIGN TIME

Requiring only the production of a single customer mask, G Series Digilin semicustom arrays offer a design cycle that the manufacturer calls both rapid and economical. Unit prices for the G Series can be under \$1 in volume production, with nonrecurring engineering charges starting at \$8,000.

The complexity of the G Series ranges from 30 logic gates, 122 transistors, and 271 resistors up to 578 logic gates, 434 transistors, and 869 resistors. A wide range of packages is available, with 8 to 44 pins.

Output currents of up to 250 mA are available on each chip, suiting the G Series for both analog and digital signal processing. High-current outputs also give the series the push to drive high current loads and operate in noisy electrical environments.

The arrays are supported through the manufacturer's Silicon Design System. The analog and digital parts of the circuit can be simulated using Spice parameters and Ferranti's Ulasim software, respectively.

Ferranti Interdesign Inc., 1500 Green Hills Rd., Scotts Valley, Calif. 95066.

Phone (408) 438-2900 [Circle 380]

CMOS ARRAYS USE LESS THAN 25 mW

The HPL-16RCX family consists of three low-power CMOS versions of industry-standard registered programmable logic arrays. They offer full pinout and functional equivalence to the bipolar 16RX series, with a 95% reduction in power consumption. This equivalence to the industry standard means that the designer can use an existing 16RX master device or Joint Electron Device Engineering Council-formatted paper tape to provide the programming pattern for the HPL-16RCX arrays.

Standby current is 150 μ A maximum, guaranteed over the full temperature range of the array. Operating current, a function of input toggle frequency, is guaranteed to be less than 5 mA/MHz; this results in an average operating power of less than 25 mW with a typical

standby power requirement of 250 μ W.

All HPL CMOS circuits are fully TTL- and CMOS-compatible. Propagation delay is specified at 125 ns maximum, guaranteed over the full military, industrial, or commercial temperature range.

The HPL-16RCX series is available now in sample and low-volume quantities; full production is scheduled for the fourth quarter of 1985. The array is available in the above temperature ranges and is housed in a ceramic DIP. Pricing in hundreds ranges from \$12.99 to \$36.07 each (for military parts with Dash-8 processing).

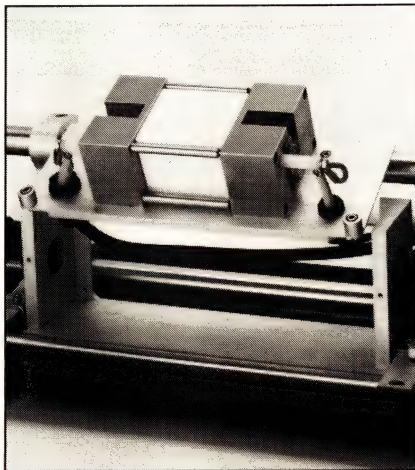
Harris Corp., Semiconductor Sector, Melbourne, Fla. 32919.

Phone (305) 727-9100 [Circle 382]

50-W LASER SYSTEM TRIMS, SCRIBES

The SL-50 continuous-wave neodymium-yttrium-aluminum-garnet (Nd:YAG) lasers are targeted at such applications as trimming, scribing, and engraving. Lasers in the series produce a multimode output of 50 W and a transverse-excitation-mode (TEM) output of 6 W at a wavelength of 1,064 nm.

An optional acousto-optical Q-switch is available for high-repetition-rate pulsed operation. The lasers are equally adapt-



able to scientific, research and development, and medical applications that require medium-power multimode or relatively high-power TEM outputs.

The SL-50 lasers consist of an optical resonator and a power station interconnected by a cable that carries electrical power and signals as well as water to cool the laser head. Incorporated in the optical resonator are the laser head, front and rear mirrors, an aperture (on TEM models), an acousto-optical Q-switch and electronic driver, and a positive-action safety shutter.

The power station, which contains the laser power supply, the cooling unit, the acousto-optical Q-switch and electronic

driver, and the control panel, can be packaged in an integral cabinet on wheels or in a 19-in. rack-mountable chassis. A remote-control unit is available as an option.

Priced from \$15,000 to \$25,000, the SL-50 lasers take 90 days for delivery. The systems are built by Spectron Laser Systems Ltd.

Meditec of America, 616 E St., Clearwater, Fla. 33516.

Phone (813) 442-8115 [Circle 383]

75-MHz DAC WORKS IN GRAPHICS SYSTEMS

Designed for high-resolution graphics systems, the Bt102 video digital-to-analog converter drives a doubly terminated 75- Ω load, allowing easy interfacing to color and monochrome monitors. With a 75-MHz conversion speed, the DAC is three times faster than other commercially available 8-bit DACs, the manufacturer says; power dissipation is just 500 mW at full-rated clock speed.

The Bt102 supports screen resolutions up to 1,024 by 800 pixels at 60-Hz frame rates. The monolithic chip is designed in CMOS silicon-gate technology and guarantees differential linearity error to be less than $\pm 1/4$ least significant bit and integral linearity error to be less than $\pm 1/2$ LSB.

Available now, the Bt102 sells for \$31 each in lots of 1,000 pieces.

Brooktree Corp., 11175 Flintkote Ave., Building F, San Diego, Calif. 92121.

Phone (619) 452-7580 [Circle 377]

INTEGRATING ADCs TOP STANDARD PARTS

The ICL7100 line of integrating analog-to-digital converters is said to better the performance of its industry-standard counterparts. Using CMOS technology, these dual-slope ADCs feature excellent differential linearity, high normal-mode rejection of power-line frequencies, virtually no zero-offset error, and a maximum-gain temperature coefficient of 5 parts per million/ $^{\circ}$ C.

Each chip has a zero integrator phase to assure fast recovery from overrange inputs, and each is also subjected to 24 to 48 h of 150 $^{\circ}$ C biased burn-in as part of the company's standard processing. The accumulated life test data shows a rate of only nine failures per billion hours at 25 $^{\circ}$ C operation. Prices for the ICL7100 family range from \$7.95 to \$14 in 100-piece quantities. Most parts are available in 40-lead ceramic DIPs and 44-lead plastic chip carriers.

Maxim Integrated Products, 510 N. Pastoria Ave., Sunnyvale, Calif. 94086.

Phone (408) 737-7600 [Circle 378]



A gas filter that needs only 1.16 by 3.00 in. is suited for semiconductor equipment such as plasma etch, chemical-vapor deposition, and diffusion processes. The Wafergard Mini in-line filter is designed to be installed downstream of mass-flow controllers and solenoid valves, in low flow-rate applications with pressures up to 2,500 psi. Wafergard Minis filter particles as small as 0.05 μm . Their stainless-steel electroplated finish gives an exceptionally clean passive surface.

Millipore Corp., 80 Ashby Rd., Bedford, Mass. 01730. Phone (800) 225-1380 (in Massachusetts, [617] 275-9200) [Circle reader service number 426]

More than 130 test and measurement technician's tools come in the models ATK-1 and ATK-2 toolkits. The kits include Phillips-head screwdrivers for #0 to #2 screws, slotted screwdrivers from $\frac{1}{8}$ by 2 in. to $\frac{1}{4}$ by 6 in., nut drivers that handle up to 9/16-in. hex nuts, 6-in. straight-nose and 5-in. long-nose pliers, diagonal cutters, and more. The tools are organized in pallet holders, in either an aluminum or a thermoplastic case. Analog and digital multimeters are available as an option. Among the models offered, the 881 measures temperatures with a type K thermocouple that gives readings in millivolts.

Omega Engineering Inc., 1 Omega Dr., Box 4047, Stamford, Conn. 06907. Phone (203) 359-1660 [Circle 422]

The Statfree CP 636 field-service kit is designed to prevent damage to components during board repair and replacement, draining electrostatic discharge from personnel, spare parts, and tools before board changes and other computer-repair jobs. The kit contains a conductive vinyl work surface, two elastic wrist bands (large and small), two

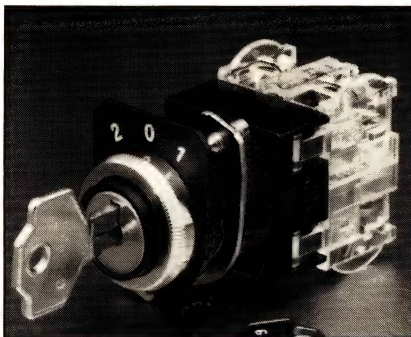
grounding cords, and a cotton storage pouch. It is designed to fit into a standard tool case.

Charleswater Products Inc., 93 Border St., West Newton, Mass. 02165. Phone (617) 964-8370 [Circle 423]

The Vyndux product line of conductive polyvinylchloride thermoplastic film and sheet provides low volume and surface resistivities with continuous and permanent static dissipation—lower than antistatic coatings, the manufacturer says. Vyndux products meet Federal Standard 101, method 4046, for minimum static decay. They are self-extinguishing in a fire, regardless of thickness. The film and sheet come in thicknesses from 10 to 60 mils, for both shallow- and deep-draw applications.

Technical Plastic Extruders Inc., 574 Ferry St., Newark, N.J. 07105. Phone (201) 589-5800 [Circle 424]

An antistatic keylock control called the series T2000 is available in two- and three-position versions with either maintained or momentary functions. The oil-tight units have Snapblock proprietary contact blocks, requiring no tools or hardware for assembly. Double-break



silver contacts come in transparent polycarbonate for easier contact inspection. The series T2000 keylocks meet many standard-circuit requirements and are suited for computer-related applications where electrostatic-discharge control is critical.

Alco Electronic Products Inc., 1551 Os-good St., North Andover, Mass. 01845. Phone (617) 685-4371 [Circle 421]

Pc-board stiffeners with tin plating that meets MIL-T-10727, type 1, requirements come in various body configurations. The stiffeners do not interfere with components, and they can provide power or ground distribution. Pin spacing is offered in any increment of 0.1, and a variety of thicknesses of the copper- or brass-alloy base are available. Custom plating is also offered.

Logic Dynamics Inc., 16918 S. Gramercy Pl., Gardena, Calif. 90247. Phone (213) 770-8151 [Circle 427]

A packaging material exceeding MIL-B-81705B standards (requiring a product to dissipate a 5,000-V charge in 2 s), Microfoam Anti-Stat protects electronic components from electrostatic discharge during shipping. Available in thicknesses from 1/16 to $\frac{1}{4}$ in., the polypropylene material has a natural sweat layer on its surface for moisture protection. The manufacturer says it also offers good thermal insulation.

Ametek, Microfoam Division, 265 Rte. 202, Chadds Ford, Pa. 19317. Phone (215) 358-1180 [Circle 425]

A single-component, die-attach epoxy, Epo-Tek H35-175, is made entirely of solids—the adhesive contains no solvents or diluents in the adhesive to cause voids in the bond line. Thus die shear on a 40-by-40-mil chip at 200°C is at least 4,500 psi. Epo-Tek H35-175 does not require refrigeration.

Epoxy Technology Inc., 14 Fortune Dr., Billerica, Mass. 01821. Phone (617) 667-3805 [Circle 431]

Ronascreen 1655 ultraviolet solder mask resists heat, moisture, abrasion, and solvents, the manufacturer says. The solder mask is easy to cure, adheres to copper or to solder with excellent line definition, and will meet MIL-STD 55110C requirements.

Learonal Inc., 272 Buffalo Ave., Freeport, N.Y. 11520. Phone (516) 868-8800 [Circle 429]

Glass substrates called Fotoform, which come in sizes up to 7 in. in diameter, can be photomachined to produce any array of through-etched holes—up to a density of 10,000/in.² This technology gives solvents maximum access to the adhesives that hold wafers in place during polishing, thus minimizing breakage when the polished wafers are removed from the substrate. Fotoform substrates are flat to within 0.0001 in. per in.

Corning Glass Works, Fotoform Products Group, MP-21-3, Corning, N.Y. 14831. Phone (607) 974-9000 [Circle 428]

Ruthenium-based thick-film resistor inks, the 6000 series offers high standards in voltage, thermal, and post-laser trim stability. For example, a trimmed 1-k Ω resistor (after 1,000 h storage at 150°C) will drift less than 0.025%, and a 100-k Ω resistor less than 0.28%. A single-phase conductive system ensures that blending is not restricted to adjacent decade values, so any two ink values in the system can be blended.

EMCA, 609 Center Ave., Mamaroneck, N.Y. 10543. Phone (914) 698-8434 [Circle 430]

BOOKS

Taxing situation. In *Tax Aspects of High Technology Operations*, the authors summarize how laws designed to accommodate old-line industries affect high-technology companies. It drew on the experience of the high-tech industry group at accountants Deloitte Haskins & Sells.

Introductory chapters present the basics of taxation. For example, a chapter on research and development, covers experimentation and software-development costs, the transfer of technology under Section 1235, and partnerships—both royalty and equity.

Tax law is still largely unwritten for software. The authors point out that defining software as an intangible (a position accepted in some state courts, though still untested in federal tax court) gives the developer opportunities to favorably interpret such points as method of accounting chosen and sales taxation. International operations occupy more than one quarter of the total text, focusing on expanding U.S. activities into other countries.

The authors succeed in keeping the language free of jargon, given that they are dealing with the Internal Revenue Code. Numerous footnotes cite the Code, case law, and the Tax Reform Act. Appendixes contain tables of Revenue Rulings, Procedures, Letter Rulings, and cases.

The inexperienced should not assume that this—or any—book is the final word on tax law. But the seasoned manager will find this \$65 volume useful. Ronald Press/John Wiley & Sons, 1 Wiley Dr., Somerset, N.J. 08873. [Circle reader service number 450]

Cause and effect. The purpose of *The Physics of Semiconductor Failures* is to provide engineering management, failure analysts, and solid-state-research engineers with information that will link the observed failure or lead loss in an IC to a specific process-induced effect. So author Howard K. Dicken presents sections on semiconductor and LSI design and processing, failure mechanisms, case histories, and corrective actions. Dicken is president of DM Data Inc. The book sells for \$145.

DM Data Inc., 6900 E. Camelback Rd., Suite 1000, Scottsdale, Ariz. 85251

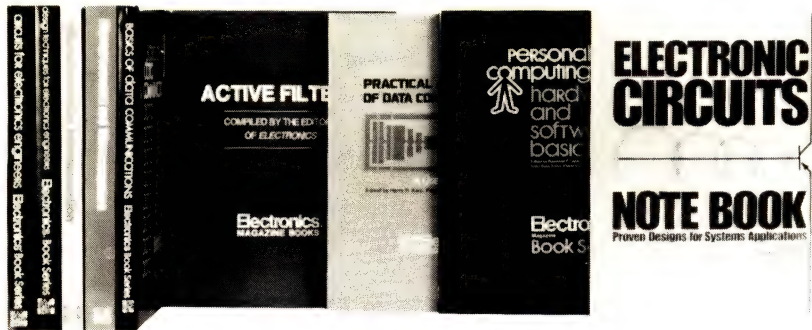
[Circle 451]

Noise analysis. *Noise in Electronic Devices and Systems*, written by M. J. Buckingham, examines the physical characteristics of noise in microwave, tunneling, and opto-electronic devices. Noise is often the limiting factor in small-signal applications.

The author bases his exposition on a

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This compilation of essential articles from *Data Communications* magazine includes chapters on terminals, acoustic couplers and modems, communications processors, networking, channel performance, data link controls, network diagnostics, interfaces, and regulations and policy. Pub. 1976, 303 pages, softcover. Order No. R-608, \$15.95.

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Electronics / July 22, 1985

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general mathematical treatment of noise processes, establishing the properties of random pulse trains and impulse processes. Thus the reader gains an overall understanding of random waveforms and becomes familiar with the intricacies of nonlinear systems and the effect of nonlinearity on noise. Each chapter ends with references.

The book, published by Ellis Horwood Ltd., sells for \$34.95.

Halsted Press/John Wiley & Sons, 605 Third Ave., New York, N.Y. 10016

[Circle 452]

LETTERS

AT&T on its 32-bit family

To the editor: We read with great interest your article on the emerging 32-bit microprocessor marketplace [*ElectronicsWeek*, June 3, 1985, p. 50]. Since we believe it is the type of article that our potential customers will clip and save, we would like to set the record straight on some facts about the AT&T 32-bit microprocessor family—the Unix Microsystem.

AT&T is in the market now with our second-generation 32-bit chips. Available in production quantities are the central processing unit, memory-management unit, math-acceleration unit, and system-interface unit. Other peripheral chips are currently being sampled.

Here are corrections for the AT&T WE32100 processor described in the column on the far right of the table on p. 52: throughput (mips) should read 2 to 3; power consumption (W), 0.8 to 1.1; instruction cache (bytes), 256; data cache (bytes), 0; addressing modes, 18; number of instructions, 181; instruction queue, 8 bytes; general-purpose registers, 9; and dedicated registers, 7.

Allan M. Hofmann, manager
Market and Sales Planning,
Microprocessors
AT&T Technology Systems
Holmdel, N.J.

CORRECTIONS

Credit for the development of the GaInAsP laser array should go to the Tokyo Institute of Technology, rather than to Japan's Tohoku University as stated in a photo caption [ElectronicsWeek, June 3, 1985, p. 30].

A caption incorrectly describes a photograph as that of Terry Leeder, vice president of Waferscale Integration Inc. of Fremont, Calif. [ElectronicsWeek, June 17, 1985, p. 43]. The photograph that appeared was of James Downey, senior vice president of operations for Advanced Micro Devices Inc., Sunnyvale, Calif. Electronics regrets the error.

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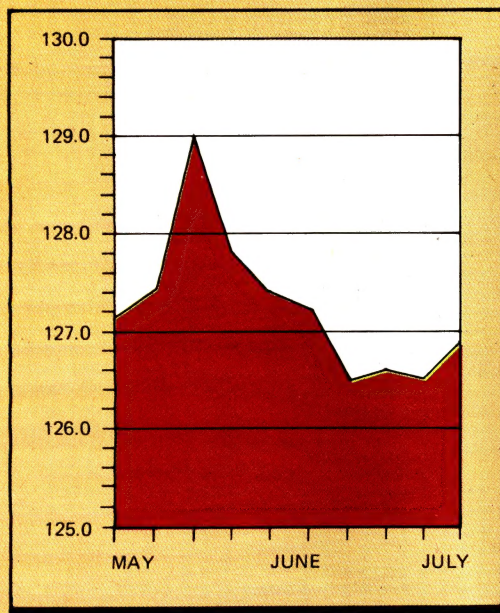
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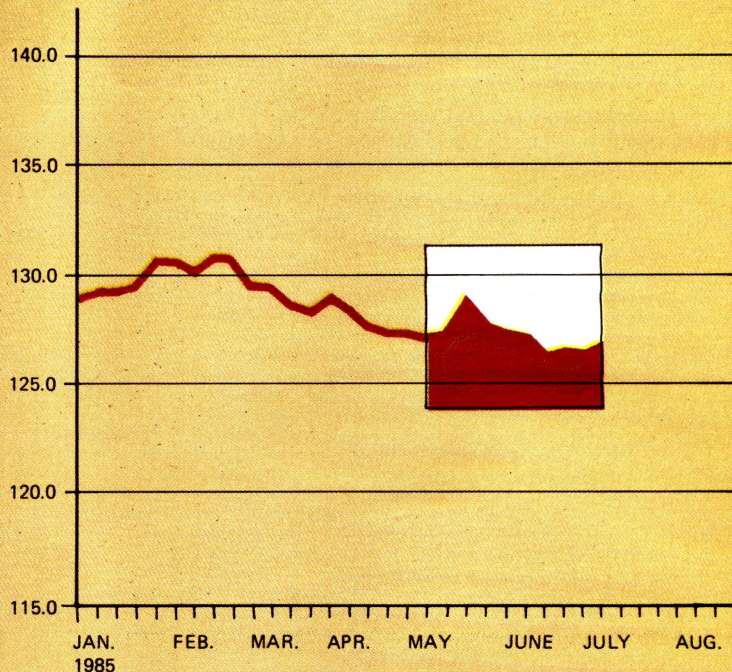
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ELECTRONICS INDEX



THIS WEEK = 126.9
 LAST WEEK = 126.5
 YEAR AGO = 126.3
 1982 = 100.0



The *Electronics Index*, a seasonally adjusted measure of the U.S. electronics industry's health, is a weighted average of various indicators. Different indicators will appear from week to week.

U.S. ELECTRONICS IMPORTS & EXPORTS (\$MILLIONS)

	IMPORTS			EXPORTS		
	May 1985	April 1985	May 1984	May 1985	April 1985	May 1984
Accounting, computing, and data-processing machines	300.963	329.794	270.036	637.633	562.275	578.646
Calculators	47.993	53.372	38.988	6.682	6.314	6.760
Parts for data-processing machines and office calculators	325.539	338.691	336.779	624.791	583.425	521.358
Telecommunications, sound-recording, and sound-reproducing equipment	1,460.503	1,650.847	1,228.633	363.261	321.971	310.428
Electronic or electric instruments	141.211	128.461	110.459	559.852	519.991	513.826
Printed-circuit boards	15.666	21.214	20.942	28.887	25.692	19.446
Integrated circuits, diodes and other semiconductors, tubes, piezoelectric crystals, parts	498.928	650.397	664.625	452.540	347.426	481.575
Fixed and variable resistors	20.139	20.869	22.906	14.530	13.100	17.101

A significant increase in exports of U.S.-made electronics products, coupled with a large decrease in imports, brought temporary relief to the *Electronics Index*. According to the most recent government statistics, the Index rose 0.3% in the latest week, an increase that reflects a surge in export strength across the board for the electronics industry during the month of May.

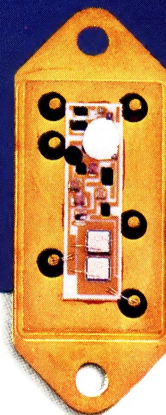
The components industry performed well for the month. Exports of semiconductors soared 30% over April's level, though they are still below the totals that were reached a year ago. At the same time, imports to the U.S. of semi-

conductors dropped 23%. Exports of resistors rose 10.9%, while shipments to overseas users of printed-circuit boards were up 12.4%. Imports of resistors and pc boards, however, fell 3.5% and 26%, respectively.

On the equipment side, exports of data-processing machines jumped 13.4% and shipments of telecommunications equipment were up 12.8%. But imports slumped 8.7% and 11.5%, respectively.

The drop in imports and the gain in exports helped to shrink the U.S. trade deficit for all electronics gear to \$120 million, a 560% improvement over April's figures.

10 Amp Power Controller



M33S shown
actual size.

**Hybrid Microelectronics — solid state power controllers
from a solid state company that you may not know exists.**

The 2" M33 Series controller shown above is only one of our microelectronic power controllers with such features as TTL/CMOS compatible inputs, optical isolation, 1553 data bus control, status feedback and power FET on-state resistance less than .02 ohms for maximum power efficiency.

And for real value added, we can also include integrated short circuit protection as well as current overload protection.

The design, manufacture and testing of hybrid microelectronics for switching and control is our technology. We have a shelf full of innovative products

for power interface, isolation and control that some companies are still trying to design.

Many are MIL QPL or per DESC selected item drawings. All can be processed and screened per MIL-STD-883 and MIL-R-28750.

We're already aboard the Space Shuttle, AWACS, the B-1 and the F-16. If you're working on a solid state power control problem — circle the number on the reader service card, write a letter, or call us. We probably have the answer — if not, we have the experience to work with you to find it.

 **TELEDYNE SOLID STATE**
A Division of Teledyne Relays

HEADQUARTERS: 12525 Daphne Avenue, Hawthorne, California 90250 • (213) 777-0077. **REGIONAL OFFICES:** Eastern Region, (201) 272-0020; Central Region, (312) 858-1090; Northwest Region, (408) 996-9944. **EUROPEAN HEADQUARTERS:** Abraham Lincoln Strasse 38-42 • 62 Wiesbaden, W. Germany 06121-7680. **U.K. SALES OFFICE:** Heathrow House, Bath Road, Cranford, Hounslow, Middlesex, TW 5 9QQ • 01-897-2501.

Circle 901 on reader service card

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There's Room in One LCD Module for the Entire Globe.

—It Displays 2,000 Characters on a Large Screen—



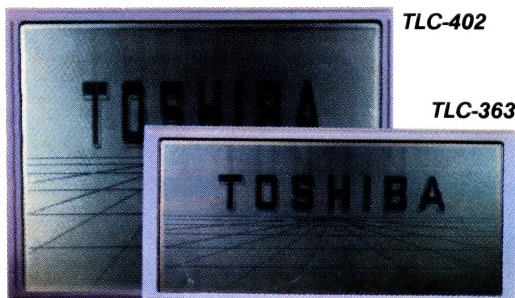
Simulated pi

New LCD modules from TOSHIBA give you 640×200 dot displays plus your choice of display area: virtually the size of an ordinary magazine or half that size.

The large display area puts a lot of information on view — either module can give you an array of 80 characters $\times$ 25 lines. Yet TOSHIBA technology cuts bulk and power consumption to the bone. These slim LCD modules are battery-powered, and they are compatible with current CRT displays without changing software.

All these features add up to portability. Versatility. Usability. These LCD modules are ideal as displays for portable word processors, personal computers, POS terminals and other display terminals.

Ask us. TOSHIBA is there when it comes to the technology you need in LCD components.



Specifications

	TLC-402	TLC-363
Display		
Number of Characters	80×25 (2,000 characters)	80×25 (2,000 characters)
Dot Format	8×8 , alpha-numeric	8×8 , alpha-numeric
Overall Dimensions (W $\times$ H $\times$ D) mm	$274.8 \times 240.6 \times 15.0$	$275.0 \times 126.0 \times 15.0$
Maximum Ratings		
Storage Temperature	$-20 - 70^{\circ}\text{C}$	$-20 - 70^{\circ}\text{C}$
Operating Temperature	$0 - 50^{\circ}\text{C}$	$0 - 50^{\circ}\text{C}$
Supply Voltage	V DD 7 V V DD-V EE 18 V	7 V 18 V
Input Voltage	$0 \leq V_{IN} \leq V_{DD}$	$V_{SS} \leq V_{IN} \leq V_{DD}$
Recommended Operating Conditions		
Supply Voltage	V DD 5 ± 0.25 V V EE -13 V Max.	5 ± 0.25 V -13 V Max.
Input Voltage	High 4.0 V Min. Low 0.5 V Max.	4.0 V Min. 0.5 V Max.
Typical Characteristics (25°C)		
Response Time	Turn ON 300 ms Turn OFF 300 ms	300 ms 300 ms
Contrast Ratio	5	5
Viewing Angle	$15 - 35$ degrees	$15 - 35$ degrees

Design and specifications are subject to change without notice.

TOSHIBA

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